

Triacs

logic level

BT131 series

GENERAL DESCRIPTION

Passivated, sensitive gate triacs in a plastic envelope, intended for use in general purpose bidirectional switching and phase control applications. These devices are intended to be interfaced directly to microcontrollers, logic integrated circuits and other low power gate trigger circuits.

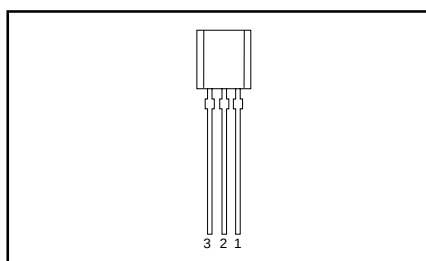
QUICK REFERENCE DATA

SYMBOL	PARAMETER	MAX.	MAX.	MAX.	UNIT
V_{DRM}	Repetitive peak off-state voltages	500	600	800	V
$I_{\text{T(RMS)}}$	RMS on-state current	1	1	1	A
I_{TSM}	Non-repetitive peak on-state current	16	16	16	A

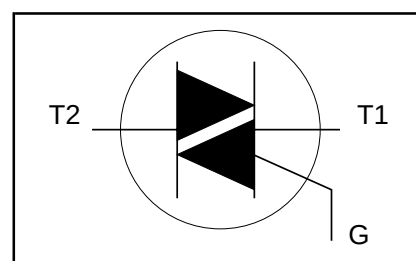
PINNING - TO92

PIN	DESCRIPTION
1	main terminal 2
2	gate
3	main terminal 1

PIN CONFIGURATION



SYMBOL



LIMITING VALUES

Limiting values in accordance with the Absolute Maximum System (IEC 134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.			UNIT
V_{DRM}	Repetitive peak off-state voltages		-	-500 500 ¹	-600 600 ¹	-800 800	V
$I_{\text{T(RMS)}}$	RMS on-state current	full sine wave; $T_{\text{lead}} \leq 51^\circ\text{C}$	-	1			A
I_{TSM}	Non-repetitive peak on-state current	full sine wave; $T_j = 25^\circ\text{C}$ prior to surge	-	16			A
		$t = 20\text{ ms}$	-	17.6			A
		$t = 16.7\text{ ms}$	-	1.28			A ² s
I^2t	I^2t for fusing	$t = 10\text{ ms}$	-	10			A/μs
di_t/dt	Repetitive rate of rise of on-state current after triggering	$I_{\text{TM}} = 1.5\text{ A}$; $I_{\text{G}} = 0.2\text{ A}$; $di_{\text{G}}/dt = 0.2\text{ A}/\mu\text{s}$	-	50			A/μs
		T2+ G+	-	50			A/μs
		T2+ G-	-	50			A/μs
		T2- G-	-	10			A/μs
		T2- G+	-	2			A
I_{GM}	Peak gate current		-	5			V
V_{GM}	Peak gate voltage		-	5			W
P_{GM}	Peak gate power		-	0.5			W
$P_{\text{G(AV)}}$	Average gate power	over any 20 ms period	-	150			°C
T_{stg}	Storage temperature		-40	125			°C
T_j	Operating junction temperature		-				

¹ Although not recommended, off-state voltages up to 800V may be applied without damage, but the triac may switch to the on-state. The rate of rise of current should not exceed 3 A/μs.

Triacs

logic level

BT131 series

THERMAL RESISTANCES

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$R_{th\ j-lead}$	Thermal resistance junction to lead	full cycle	-	-	60	K/W
$R_{th\ j-a}$	Thermal resistance junction to ambient	half cycle	-	-	80	K/W
		pcb mounted; lead length = 4mm	-	150	-	K/W

STATIC CHARACTERISTICS

$T_j = 25\ ^\circ\text{C}$ unless otherwise stated

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
I_{GT}	Gate trigger current	$V_D = 12\ \text{V}$; $I_T = 0.1\ \text{A}$	-	-	-	-
		T2+ G+	-	0.4	3	mA
		T2+ G-	-	1.3	3	mA
		T2- G-	-	1.4	3	mA
		T2- G+	-	3.8	7	mA
I_L	Latching current	$V_D = 12\ \text{V}$; $I_{GT} = 0.1\ \text{A}$	-	-	-	-
		T2+ G+	-	1.2	5	mA
		T2+ G-	-	4.0	8	mA
		T2- G-	-	1.0	5	mA
		T2- G+	-	2.5	8	mA
I_H	Holding current	$V_D = 12\ \text{V}$; $I_{GT} = 0.1\ \text{A}$	-	1.3	5	mA
V_T	On-state voltage	$I_T = 2.0\ \text{A}$	-	1.2	1.5	V
V_{GT}	Gate trigger voltage	$V_D = 12\ \text{V}$; $I_T = 0.1\ \text{A}$	-	0.7	1.5	V
		$V_D = 400\ \text{V}$; $I_T = 0.1\ \text{A}$; $T_j = 125\ ^\circ\text{C}$	0.2	0.3	-	V
I_D	Off-state leakage current	$V_D = V_{DRM(max)}$; $T_j = 125\ ^\circ\text{C}$	-	0.1	0.5	mA

DYNAMIC CHARACTERISTICS

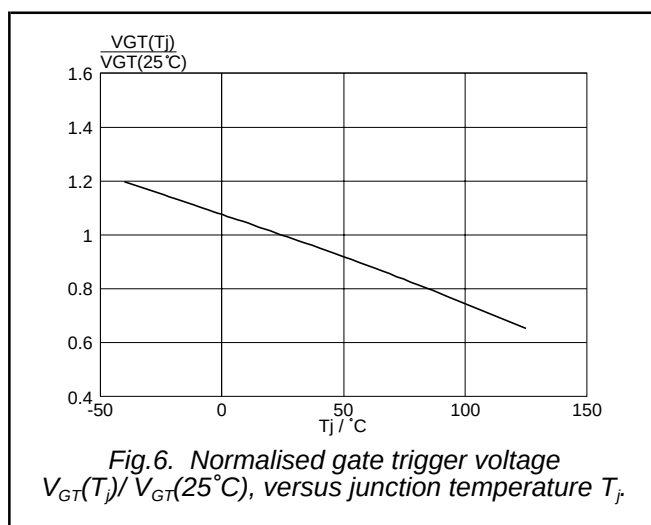
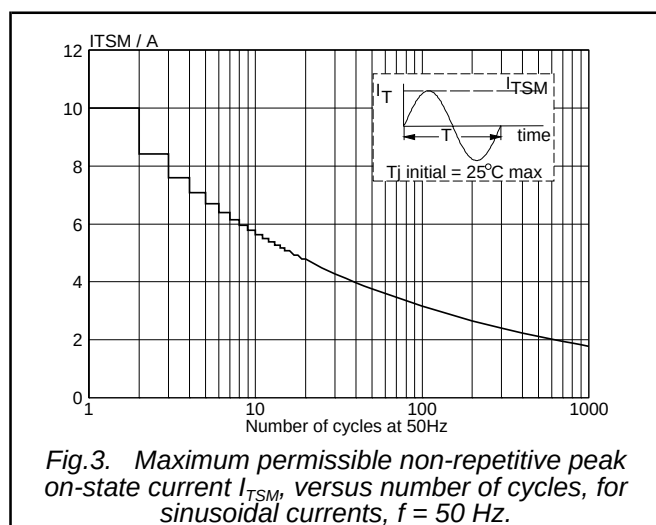
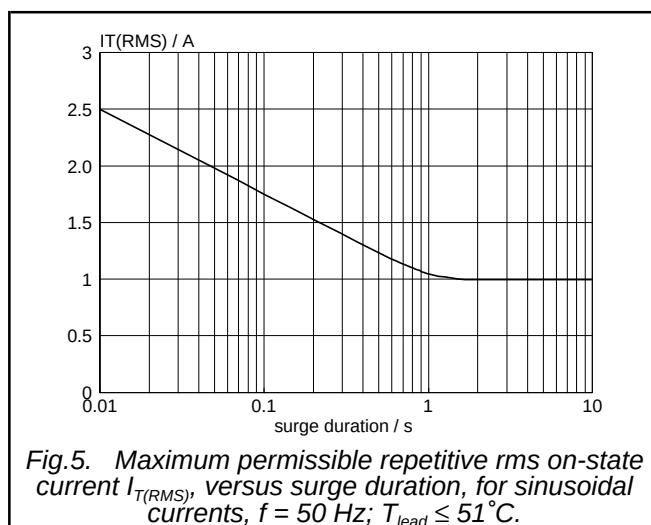
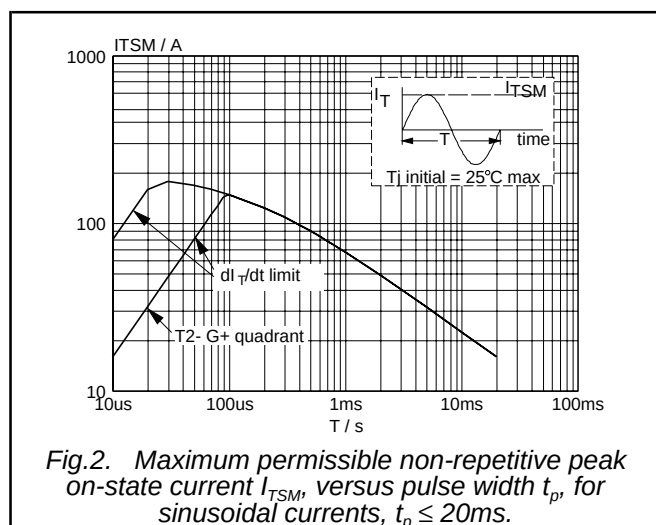
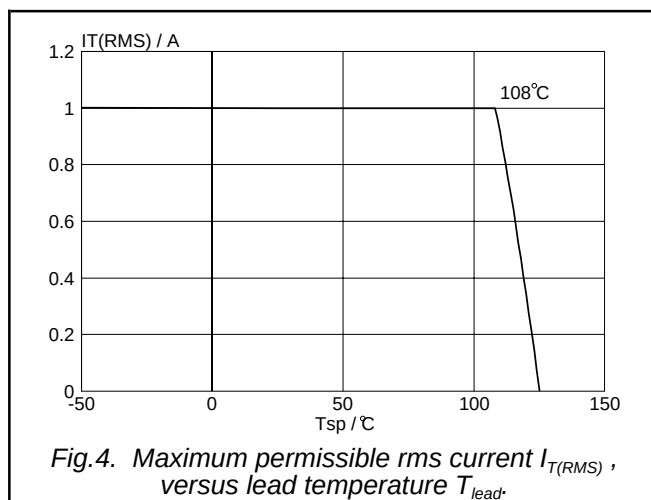
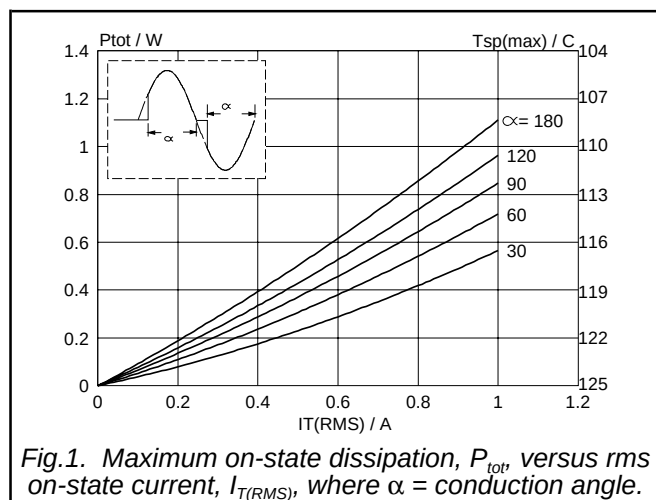
$T_j = 25\ ^\circ\text{C}$ unless otherwise stated

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
dV_D/dt	Critical rate of rise of off-state voltage	$V_{DM} = 67\% V_{DRM(max)}$; $T_j = 125\ ^\circ\text{C}$; exponential waveform; $R_{GK} = 1\ \text{k}\Omega$	5	15	-	V/ μs
t_{gt}	Gate controlled turn-on time	$I_{TM} = 1.5\ \text{A}$; $V_D = V_{DRM(max)}$; $I_G = 0.1\ \text{A}$; $di_G/dt = 5\ \text{A}/\mu\text{s}$	-	2	-	μs

Triacs

logic level

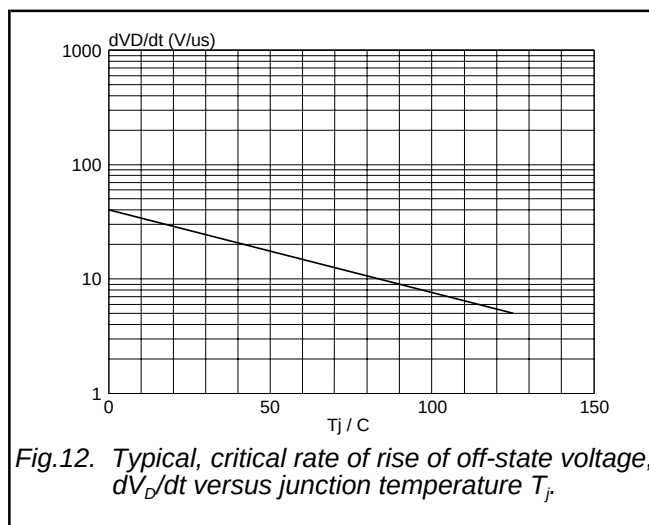
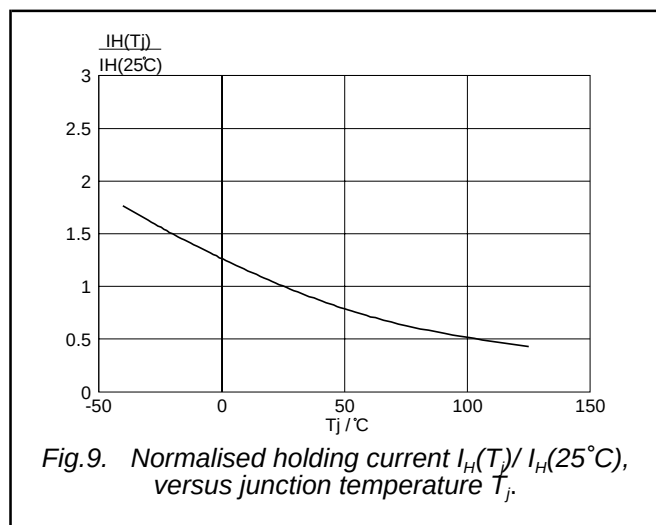
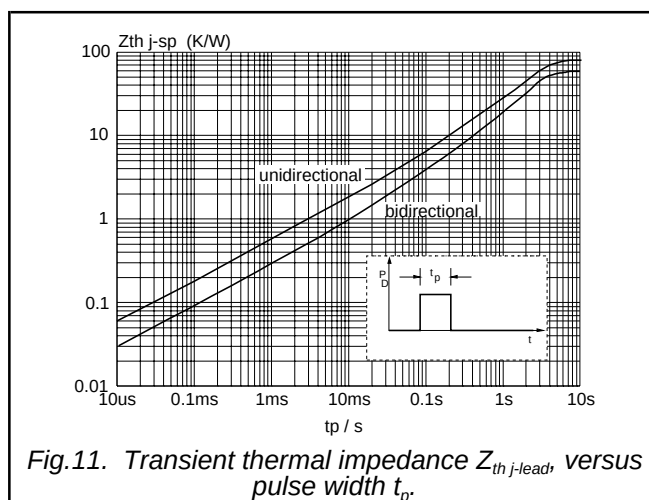
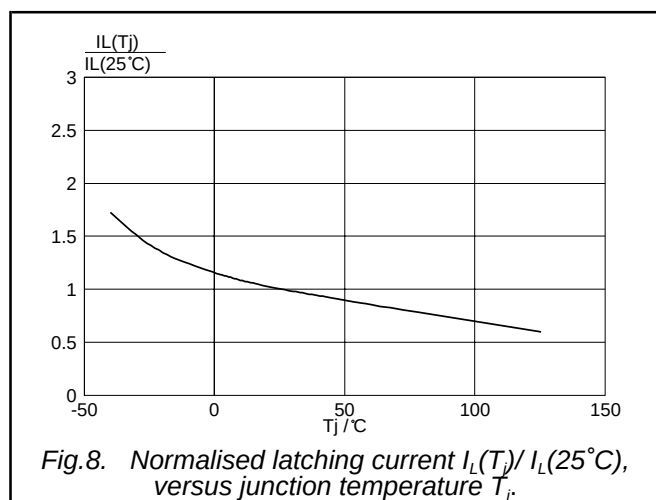
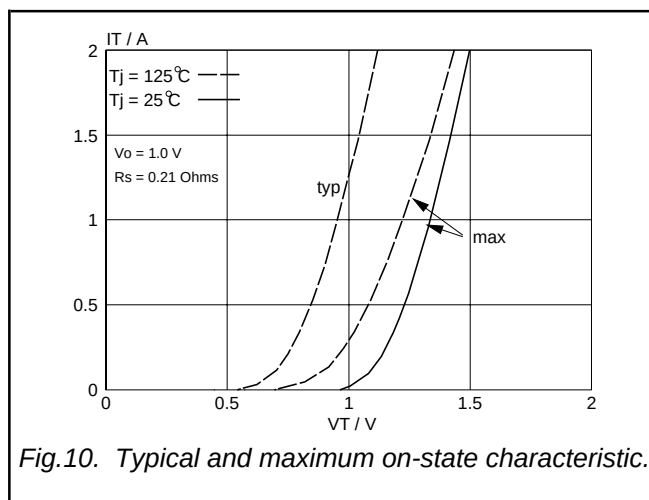
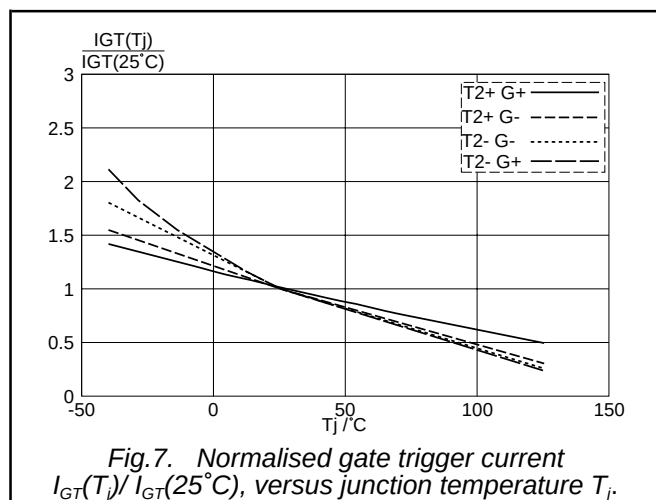
BT131 series



Triacs

logic level

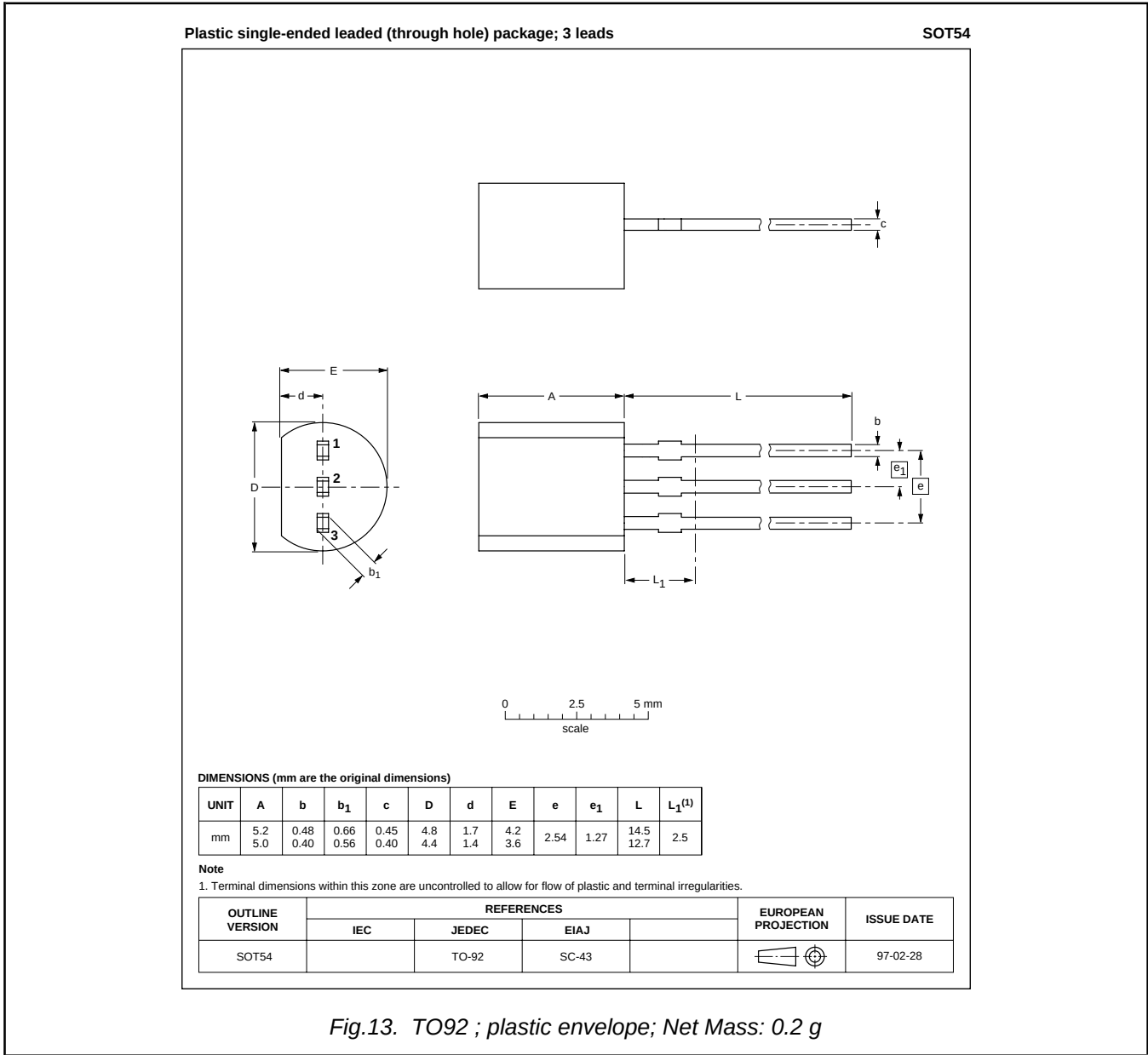
BT131 series



Triacs
logic level

BT131 series

MECHANICAL DATA



Notes

1. Epoxy meets UL94 V0 at 1/8".