

DATA SHEET

TDA4850

Horizontal and vertical deflection
controller for VGA/XGA and
multi-frequency monitors

Product specification
Supersedes data of September 1991
File under Integrated Circuits, IC02

1997 Jun 05

Horizontal and vertical deflection controller for VGA/XGA and multi-frequency monitors

TDA4850

FEATURES

- VGA operation fully implemented including alignment-free vertical and E/W amplitude pre-settings
- 4th VGA mode easy applicable (XGA, Super VGA)
- Multi-frequency operation externally selectable
- All adjustments DC-controllable
- Alignment-free oscillators
- Sync separators for video or horizontal and vertical TTL sync levels regardless of polarity
- Horizontal oscillator with PLL1 for sync and PLL2 for flyback
- Constant vertical and E/W amplitude in multi-frequency operation
- DC-coupling to vertical power amplifier (TDA486X or TDA8351)
- Internal supply voltage stabilization with excellent ripple rejection to ensure stable geometrical adjustments.

GENERAL DESCRIPTION

The TDA4850 provides economical solutions in VGA/XGA and multi-frequency monitors. The IC incorporates the complete horizontal and vertical small signal processing. VGA-dependent mode detection and settings are performed on chip. In conjunction with TDA486X or TDA8351 (vertical output circuits) both ICs offer an extremely advanced system solution.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V_P	supply voltage (pin 1)	9.2	12	16	V
I_P	supply current	–	40	–	mA
$V_{i\ sync}$	AC-coupled composite video signal with negative-going sync (peak-to-peak value; pin 9)	–	1	–	V
	sync slicing level	–	120	–	mV
	DC-coupled TTL-compatible horizontal sync signal (peak value; pin 9)	1.7	–	–	V
	slicing level	1.2	1.4	1.6	V
	DC-coupled TTL-compatible vertical sync signal (peak value; pin 10)	1.7	–	–	V
	slicing level	1.2	1.4	1.6	V
I_{oV}	vertical differential output current (peak-to-peak value; pins 5 and 6)	–	1	–	mA
I_{oH}	horizontal sink output current on pin 3	–	–	60	mA
T_{amb}	operating ambient temperature	0	–	70	°C

ORDERING INFORMATION

TYPE NUMBER	PACKAGE		
	NAME	DESCRIPTION	VERSION
TDA4850	DIP20	plastic dual in-line package; 20 leads (300 mil)	SOT146-1

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BLOCK DIAGRAM

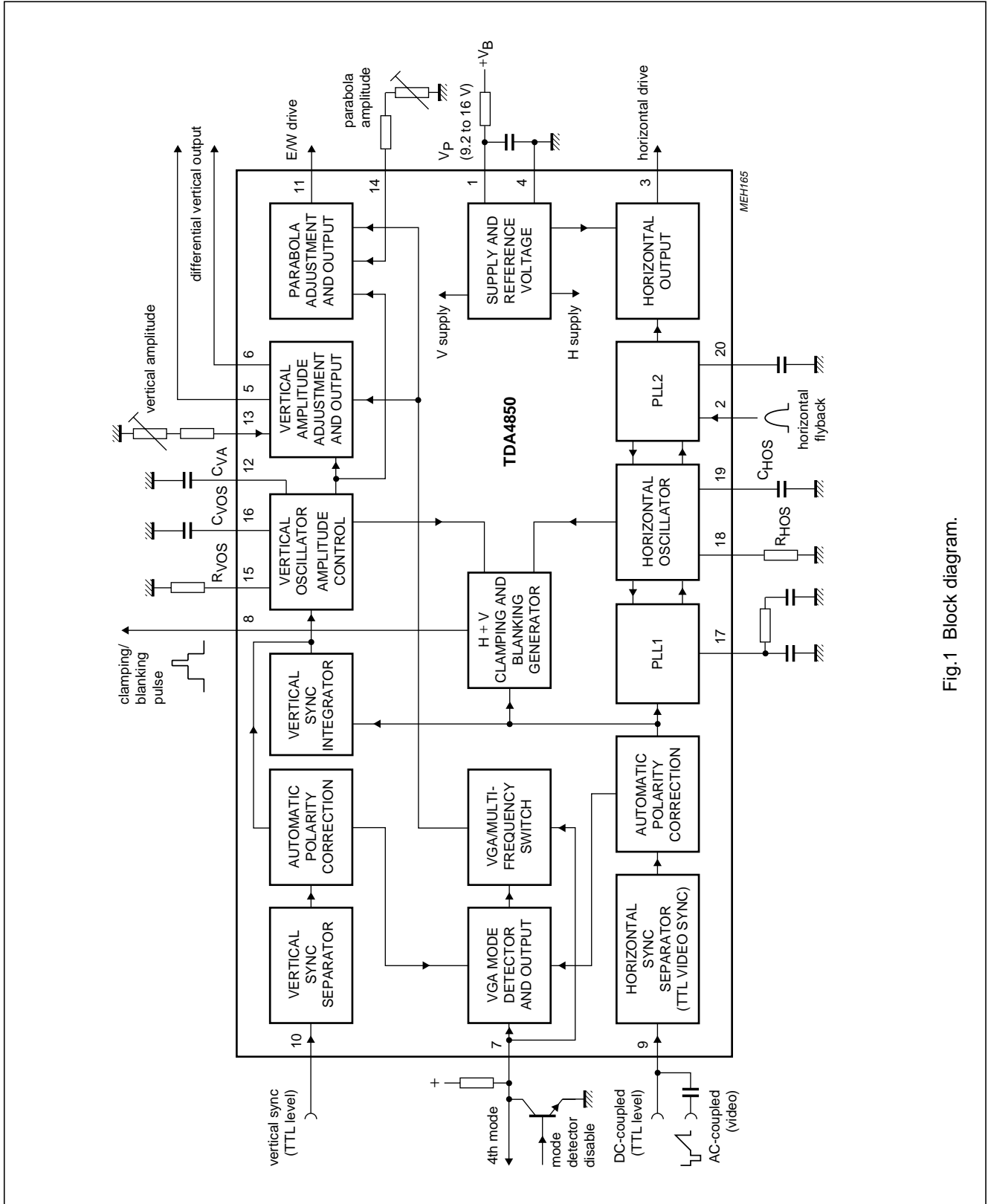


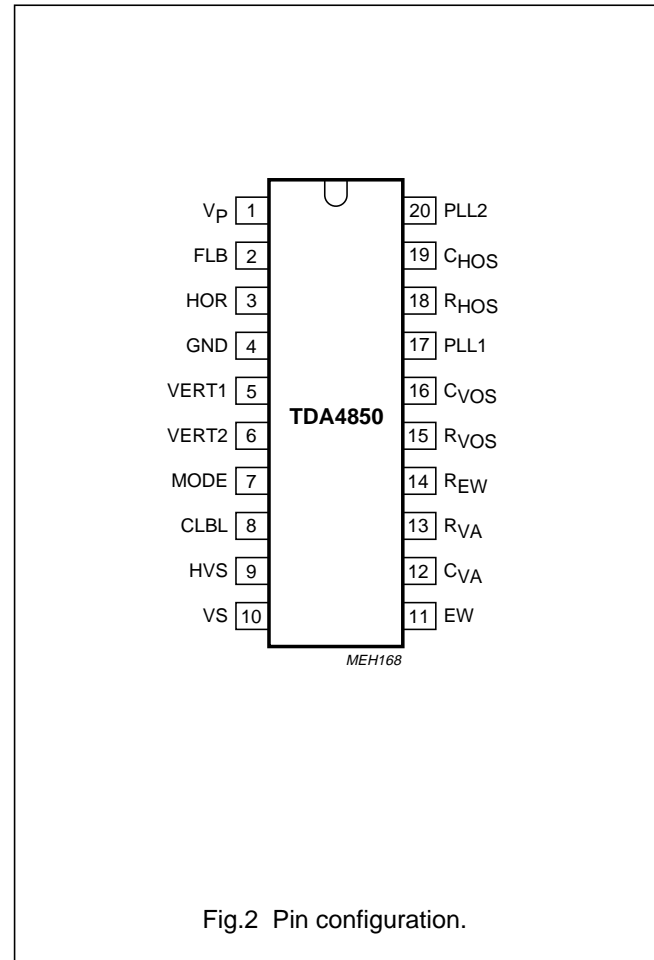
Fig.1 Block diagram.

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PINNING

SYMBOL	PIN	DESCRIPTION
V _P	1	positive supply voltage
FLB	2	horizontal flyback input
HOR	3	horizontal output
GND	4	ground (0 V)
VERT1	5	vertical output 1; negative-going sawtooth
VERT2	6	vertical output 2; positive-going sawtooth
MODE	7	4th mode output and mode detector disable input
CLBL	8	clamping/blanking pulse output
HVS	9	horizontal sync/video input
VS	10	vertical sync input
EW	11	E/W output (parabola to driver stage)
C _{VA}	12	capacitor for amplitude control
R _{VA}	13	vertical amplitude adjustment input
R _{EW}	14	E/W amplitude adjustment input (parabola)
R _{VOS}	15	vertical oscillator resistor
C _{VOS}	16	vertical oscillator capacitor
PLL1	17	PLL1 phase
R _{HOS}	18	horizontal oscillator resistor
C _{HOS}	19	horizontal oscillator capacitor
PLL2	20	PLL2 phase



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FUNCTIONAL DESCRIPTION

Horizontal sync separator and polarity correction

An AC-coupled video signal or a DC-coupled TTL sync signal (H only or composite sync) is input on pin 9. Video signals are clamped with top sync on 1.28 V, and are sliced at 1.4 V. This results in a fixed absolute slicing level of 120 mV related to top sync.

DC-coupled TTL sync signals are also sliced at 1.4 V, however with the clamping circuit in current limitation. The polarity of the separated sync is detected by internal integration of the signal, then the polarity is corrected.

The polarity information is fed to the VGA mode detector. The corrected sync is input signal for the vertical sync integrator and the PLL1 stage.

Vertical sync separator, polarity correction and vertical sync integrator

DC-coupled vertical TTL sync signals may be applied to pin 10. They are sliced at 1.4 V. The polarity of the separated sync is detected by internal integration, then polarity is corrected. The polarity information is fed to the VGA mode detector. If pin 10 is not used, it must be connected to ground.

The separated $V_{i(sync)}$ signal from pin 10, or the integrated composite sync signal from pin 9 (TTL or video) triggers directly the vertical oscillator.

VGA mode detector and mode output

The three standard VGA modes and a 4th not fixed mode are decoded by the polarities of the horizontal and the vertical sync input signals. An external resistor (from V_P to pin 7) is necessary to match this function. In all three VGA modes the correct amplitudes are activated. The presence of the 4th mode is indicated by HIGH on pin 7. This signal can be used externally to switch any horizontal or vertical parameters.

VGA mode detector input

For multi-frequency operation the voltage on pin 7 must be externally forced to a level of <50 mV. Vertical amplitude pre-settings for VGA are then inhibited. The delay time between vertical trigger pulse and the start of vertical deflection changes from 575 to 300 μ s (575 μ s is needed for VGA). The vertical amplitude then remains constant in a frequency range from 50 to 110 Hz.

Clamping and blanking generator

A combined clamping and blanking pulse is available on pin 8 (suitable for the video preamplifier TDA4880). The lower level of 2.1 V can be the blanking signal derived from line flyback, or the vertical blanking pulse from the internal vertical oscillator.

Vertical blanking equals to the delay between vertical sync and start of vertical scan. By this, an optimum blanking is achieved for VGA/XGA as well as for multi-frequency operation (selectable via pin 7).

The upper level of 3.9 V is the horizontal clamping pulse with internally fixed pulse width of 1 μ s. A mono flop, which is triggered by the trailing edge of the horizontal sync pulse, generates this pulse.

PLL1 phase detector

The phase detector is a standard one using switched current sources. The middle of the sync is compared with a fixed point of the oscillator sawtooth voltage. The PLL filter is connected to pin 17.

Horizontal oscillator

This oscillator is a relaxation type oscillator. Its frequency is determined mainly by the capacitor on pin 19. A frequency range of one octave is achieved by the current on pin 18. The ϕ_1 control voltage from pin 17 is fed via a buffer amplifier and an attenuator to the current reference pin 18 to achieve a high DC loop gain. Therefore, changes in frequency will not affect the phase relationship between horizontal sync pulses and line flyback pulses.

PLL2 phase detector

This phase detector is similar to the PLL1 phase detector. Line flyback signals (pin 2) are compared with a fixed point of the oscillator sawtooth voltage. Delays in the horizontal deflection circuit are compensated by adjusting the phase relationship between horizontal sync and horizontal output pulses.

A certain amount of phase adjustments is possible by injecting a DC current from an external source into the PLL2 filter capacitor on pin 20.

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Horizontal driver

This open-collector output stage (pin 3) can directly drive an external driver transistor. The saturation voltage is 300 mV at 20 mA. To protect the line deflection transistor, the horizontal output stage does not conduct at $V_P < 6.4$ V (pin 1).

Vertical oscillator and amplitude control

This stage is designed for fast stabilization of the vertical amplitude after changes in sync conditions. The free-running frequency f_o is determined by the values of R_{VOS} and C_{VOS} . The recommended values should be altered marginally only to preserve the excellent linearity and noise performance. The vertical drive currents I_5 and I_6 are in relation to the value of R_{VOS} . Therefore, the oscillator frequency must be determined only by C_{VOS} on pin 16.

$$f_o = \frac{1}{10.8 \times R_{VOS} \times C_{VOS}}$$

To achieve a stabilized amplitude the free-running frequency f_o (without adjustment) must be lower than the lowest occurring sync frequency. The contributions shown in Table 1 can be assumed.

Table 1 Calculation of f_o total spread

CONTRIBUTING ELEMENTS	%
Minimum frequency offset between f_o and the lowest trigger frequency	10
Spread of IC	± 3
Spread of R (22 k Ω)	± 1
Spread of C (0.1 μ F)	± 5
Total	19

Result for 50 to 110 Hz application: $f_o = \frac{50 \text{ Hz}}{1.19} = 42 \text{ Hz}$

Table 2 VGA modes

MODE	HORIZONTAL/VERTICAL SYNC POLARITY	HORIZONTAL FREQUENCY (kHz)	VERTICAL FREQUENCY (Hz)	NUMBER OF ACTIVE LINES	MODE OUTPUT PIN 7
1	+/-	31.45	70	350	LOW
2	-/+	31.45	70	400	LOW
3	-/-	31.45	60	480	LOW
4	+/+	fixed by external circuitry	-	-	HIGH

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LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_P	supply voltage (pin 1)		-0.5	+16	V
$V_{3,7}$	voltage on pins 3 and 7		-0.5	+16	V
V_8	voltage on pin 8		-0.5	+7	V
V_n	voltage on pins 5, 6, 9, 10, 13, 14 and 18		-0.5	+6.5	V
I_2	current on pin 2		-	±10	mA
I_3	current on pin 3		-	100	mA
I_7	current on pin 7		-	20	mA
I_8	current on pin 8		-	-10	mA
T_{amb}	operating ambient temperature		0	70	°C
T_j	junction temperature		-	150	°C
T_{stg}	storage temperature		-55	+150	°C
V_{esd}	electrostatic handling for all pins	note 1	-	±300	V

Note

1. Equivalent to discharging a 200 pF capacitor through a 0 Ω series resistor.

THERMAL CHARACTERISTICS

SYMBOL	PARAMETER	CONDITIONS	VALUE	UNIT
$R_{th(j-a)}$	thermal resistance from junction to ambient	in free air	65	K/W

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CHARACTERISTICS

$V_P = 12\text{ V}$; $T_{\text{amb}} = 25\text{ °C}$; measurements taken in Fig.6; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Supply						
V_P	supply voltage (pin 1)		9.2	12	16	V
I_P	supply current		–	40	–	mA
Internal reference voltage						
V_{ref}	internal reference voltage		6.0	6.25	6.5	V
TC	temperature coefficient	$T_{\text{amb}} = 20\text{ to }100\text{ °C}$	–	–	± 90	$10^{-6}/\text{K}$
PSRR	power supply ripple rejection	$f = 1\text{ kHz sine wave}$	60	75	–	dB
		$f = 1\text{ MHz sine wave}$	25	35	–	dB
V_P	supply voltage (pin 1) to ensure all internal reference voltages		9.2	–	16	V
Composite sync input (AC-coupled; $V_{10} = 5\text{ V}$)						
$V_{i\text{ sync}}$	sync amplitude of video input signal (pin 9)	sync on green; $R_S = 50\ \Omega$	–	300	–	mV
	top sync clamping level		1.1	1.32	1.5	V
	slicing level above top sync level		90	120	150	mV
R_S	allowed source resistance for 7% duty cycle	$V_{i\text{ sync}} > 200\text{ mV}$	–	–	1.5	$k\Omega$
r_g	differential input resistance	during sync	–	80	–	Ω
I_g	charging current of coupling capacitor	$V_g > 1.5\text{ V}$	1.7	2.6	3.4	μA
t_{int}	vertical sync integration time to generate sync pulse		7	10	13	μs
Horizontal sync input (DC-coupled, TTL-compatible)						
$V_{i\text{ sync}}$	sync input signal (peak value; pin 9)		1.7	–	–	V
	slicing level		1.2	1.4	1.6	V
t_p	minimum pulse width		700	–	–	ns
t_r, t_f	rise time and fall time		10	–	500	ns
I_g	input current	$V_g = 0.8\text{ V}$	–	–	–200	μA
		$V_g = 5.5\text{ V}$	–	–	10	μA
Automatic horizontal polarity switch (H-sync on pin 9)						
$t_{p\text{ H}/t_{\text{H}}}$	horizontal sync pulse width related to t_{H} (duty cycle for automatic polarity correction)		–	–	30	%
t_p	delay time for changing sync polarity		0.3	–	1.8	ms
Vertical sync input (DC-coupled, TTL-compatible; V-sync on pin 10)						
$V_{i\text{ sync}}$	sync input signal (peak value; pin 10)		1.7	–	–	V
	slicing level		1.2	1.4	1.6	V
I_{10}	input current	$0 < V_{10} < 5.5\text{ V}$	–	–	± 10	μA
$t_{p\text{ V}}$	maximum vertical sync pulse width for automatic vertical polarity switch		–	–	300	μs

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SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Horizontal mode detector output (VGA mode)						
V ₇	output saturation voltage LOW (for modes 1, 2 and 3)	I ₇ = 6 mA	–	0.275	0.33	V
	output voltage HIGH	mode 4	–	–	V _P	V
I ₇	load current to force VGA mode-dependent vertical and parabola amplitudes	modes 1, 2 and 3	2	–	6	mA
	output current	mode 4	–	0	–	mA
VGA/multi-frequency mode switch						
V ₇	input voltage LOW to force multi-frequency mode		0	–	50	mV
Horizontal comparator PLL1						
V ₁₇	upper control voltage limitation		–	5.0	–	V
	lower control voltage limitation		–	1.2	–	V
I ₁₇	control current	see Fig.3	–	±300	–	µA
Horizontal oscillator						
f _{osc}	centre frequency	R ₁₈ = 12 kΩ (pin 18); C ₁₉ = 2.2 nF (pin 19)	–	31.45	–	kHz
Δf _{osc}	deviation of centre frequency		–	–	±3.0	%
TC	temperature coefficient		–	–	±150	10 ⁻⁶ /K
φ _H /t _H	relative holding/catching range		±6	±6.5	±7.3	%
R ₁₈	external oscillator resistor		9	–	18	kΩ
V ₁₈	voltage at reference current input (pin 18)	PLL1 and PLL2 locked; V _{ref} = 6.25 V	–	3.125	–	V
ΔV ₁₈	control voltage		–	±205	–	mV
Horizontal PLL2; see Fig.3						
V ₂	upper clamping level of flyback input	I ₂ = 6 mA	–	5.5	–	V
	lower clamping level of flyback input	I ₂ = –1 mA	–	–0.75	–	V
	H-flyback slicing level		–	3.0	–	V
I ₂	input current	H-scan; V ₈ < 0.9 V	–0.5	–	–	mA
		H-flyback; V ₈ > 1.8 V	–	–	–0.2	mA
t _d /t _H	delay between middle of sync and middle of H-flyback related to t _H		–	3.2	–	%
V ₂₀	upper control voltage limitation		–	4.6	–	V
	lower control voltage limitation		–	1.6	–	V
I ₂₀	control current		–	±200	–	µA
Δt/t _H	PLL2 control range related to t _H		30	–	–	%

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SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Horizontal output (open-collector); see Fig.3						
V ₃	output voltage LOW	I ₃ = 20 mA	–	–	0.3	V
		I ₃ = 60 mA	–	–	0.8	V
t _p /t _H	t _H duty cycle		42	45	48	%
V _P	threshold to activate too low supply voltage protection	horizontal output off	–	5.3	–	V
		horizontal output on	–	5.6	–	V
Horizontal clamping/blanking generator output; see Fig.3						
V ₈	output voltage LOW	H and V scanning	–	–	0.9	V
	blanking output voltage	internal V blanking	1.8	2.1	2.4	V
		external H blanking	1.8	2.1	2.4	V
	clamping output voltage	H-sync on pin 9	3.5	3.9	4.3	V
I ₈	internal sink current for all output levels	H and V scanning	2.3	2.9	3.5	mA
t ₈	clamping pulse start		with end of H-sync			
t _{clp}	clamping pulse width		0.8	1.0	1.2	μs
S	steepness of rise and fall times		–	40	–	ns/V
Vertical oscillator (V_{ref} = 6.25 V)						
f ₀	vertical free-running frequency	R ₁₅ = 22 kΩ; C ₁₆ = 0.1 μF	40	42	43.3	Hz
f _V	nominal vertical sync range	no f ₀ adjustment	50	–	110	Hz
V ₁₅	voltage on pin 15	R ₁₅ = 22 kΩ	2.8	3.0	3.2	V
t _d	delay between sync pulse and start of vertical scan in VGA/XGA mode, activated by an external resistor on pin 7 in multi-frequency mode	measured on pin 8				
			500	575	650	μs
		V ₇ < 50 mV	240	300	360	μs
I ₁₂	control current for amplitude control		–	±200	–	μA
C ₁₂	capacitor for amplitude control		–	–	0.33	μF
Vertical differential output; see Fig.4						
I _o	differential output current between pins 5 and 6 (peak-to-peak value)	mode 3; I ₁₃ > –135 μA; R ₁₅ = 22 kΩ	0.9	1.0	1.1	mA
	maximum offset current error	I _o = 1 mA	–	–	±2.5	%
	maximum linearity error		–	–	±1.5	%

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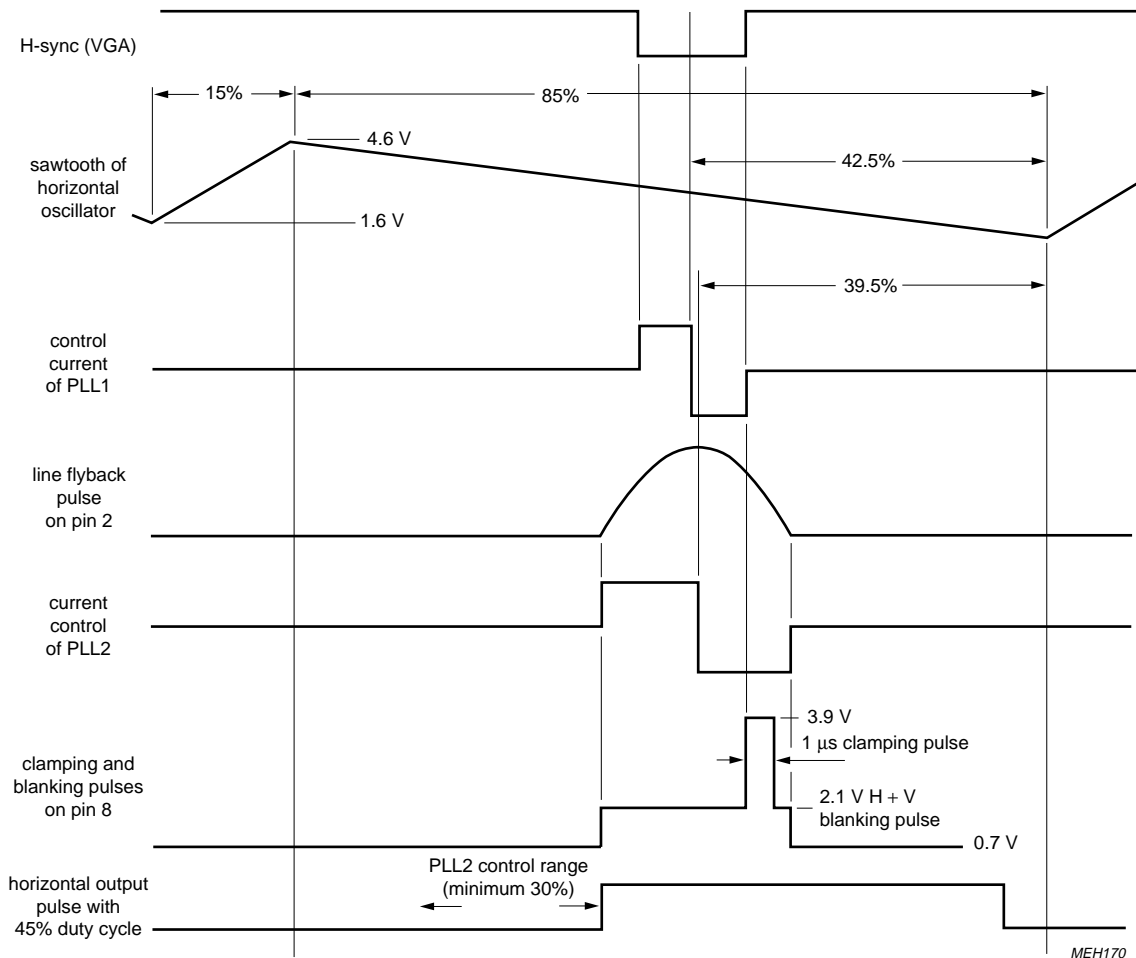
SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Vertical amplitude adjustment (in percent of output signal)						
V ₁₃	input voltage		–	5.0	–	V
I ₁₃	adjustment current	I _{o max} (100%)	–110	–120	–135	μA
		I _{o min} (typically 58%)	–	0	–	μA
ΔI _o /Δt	VGA mode-dependent pre-settings activated by an external resistor on pin 7	note 1; see Table 2				
	mode 1		116.1	116.8	117.5	%
	mode 2		102.0	102.2	102.5	%
	mode 3		–	100	–	%
	mode 4		–	100	–	%
	multi-frequency operation (VGA operation disabled)	V ₇ < 50 mV	–	100	–	%
E/W output; note 2						
V ₁₁	bottom output signal during mid-scan (pin 11)	internally stabilized	1.05	1.2	1.35	V
	top output signal during flyback		4.1	4.35	4.6	V
TC	temperature coefficient of output signal		–	–	250	10 ⁻⁶ /K
E/W amplitude adjustment (parabola); see Fig.4						
V ₁₄	input voltage (pin 14)		–	5.0	–	V
I ₁₄	adjustment current	100% parabola	–110	–120	–135	μA
		typically 28% parabola	–	0	–	μA

Notes to the Characteristics

1. ΔI_o/Δt relative to value of mode 3.
2. Parabola amplitude tracks with mode-dependent vertical amplitude but not with vertical amplitude adjustment. Tracking can be achieved by a resistor from vertical amplitude potentiometer to pin 14.

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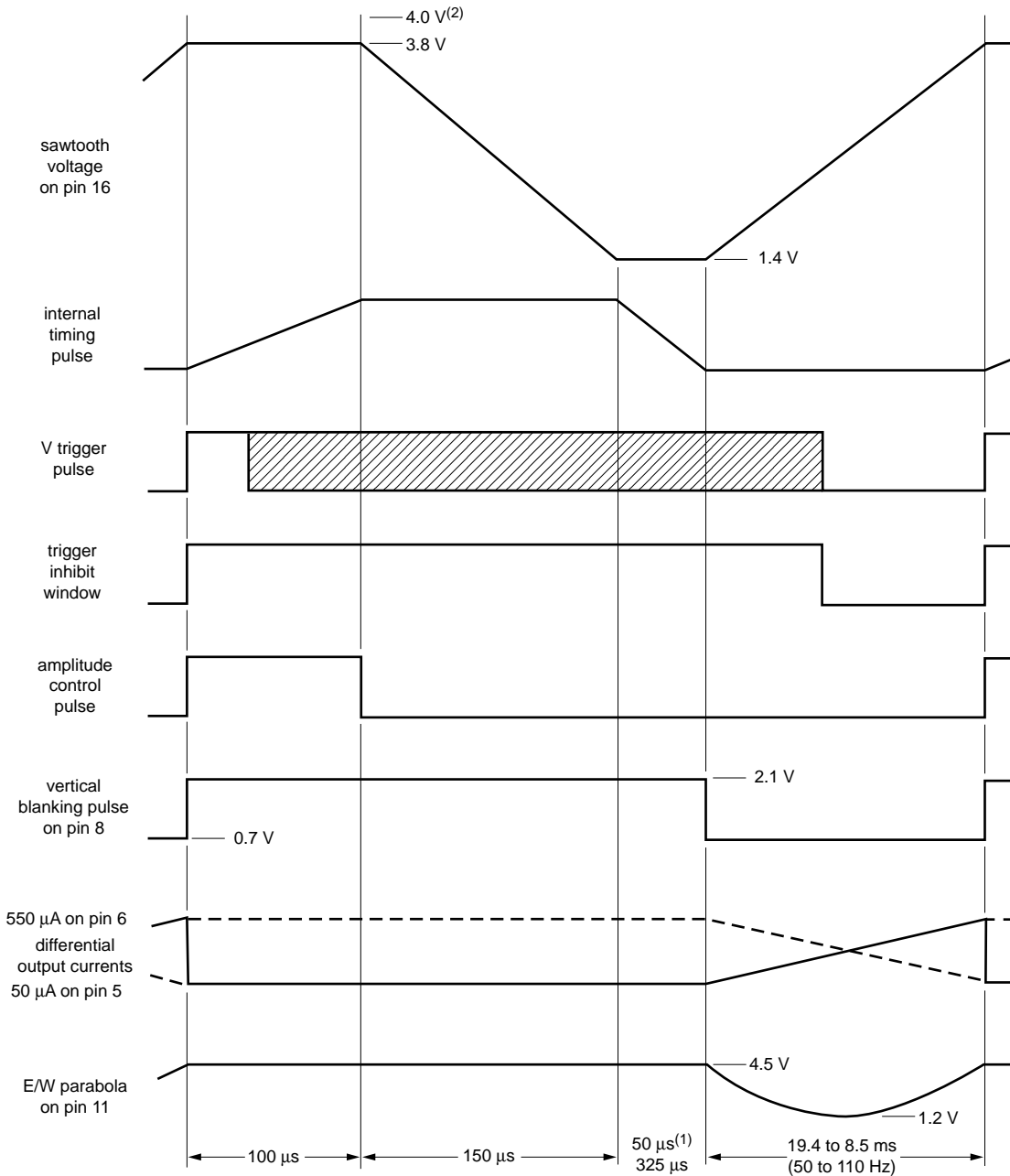


MEH170

Fig.3 Horizontal timing diagram.

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MHA711

(1) In multi-frequency mode.
(2) For free-running oscillator.

Fig.4 Vertical and E/W timing diagram.

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INTERNAL CIRCUITRY

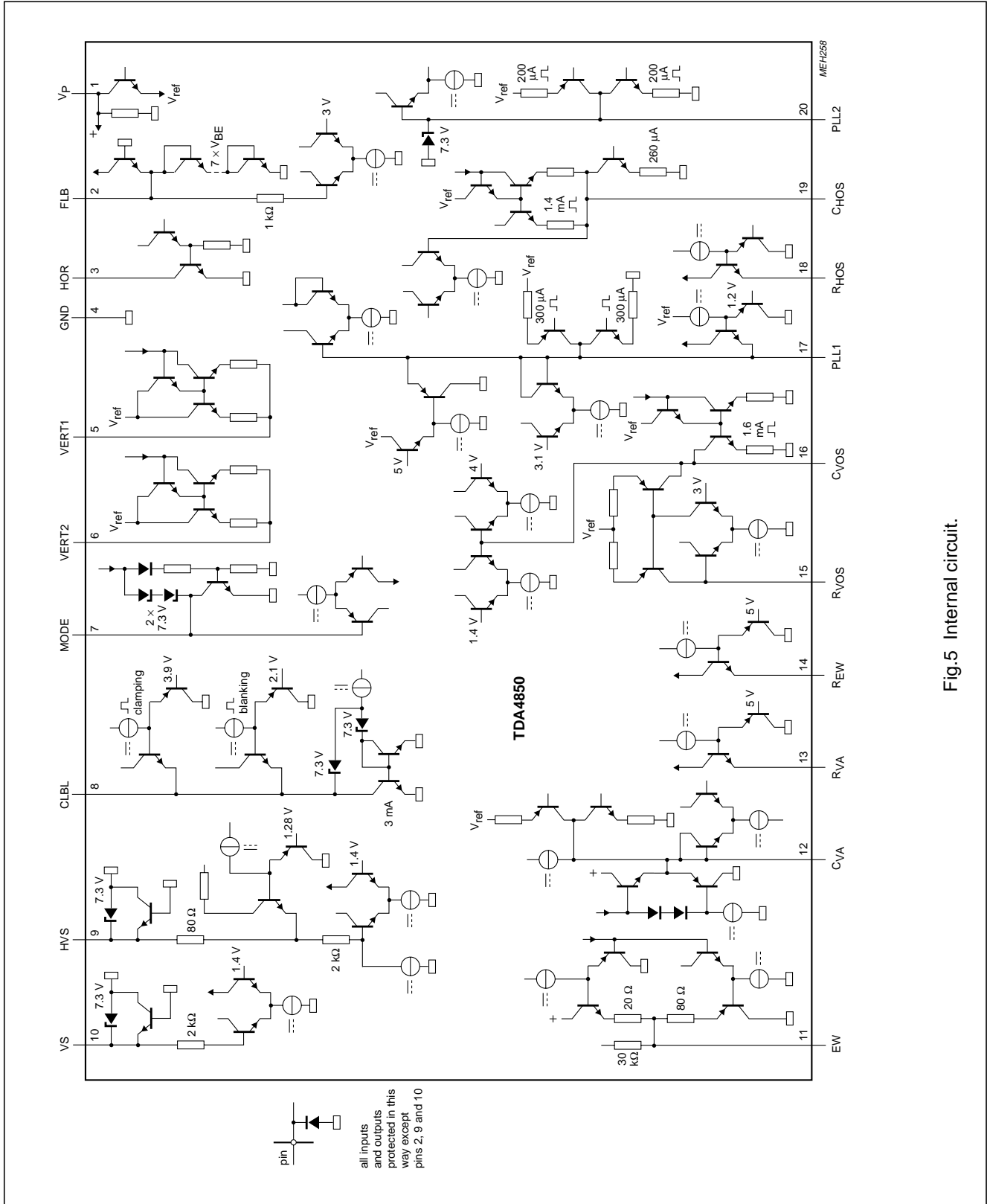


Fig.5 Internal circuit.

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TEST AND APPLICATION INFORMATION

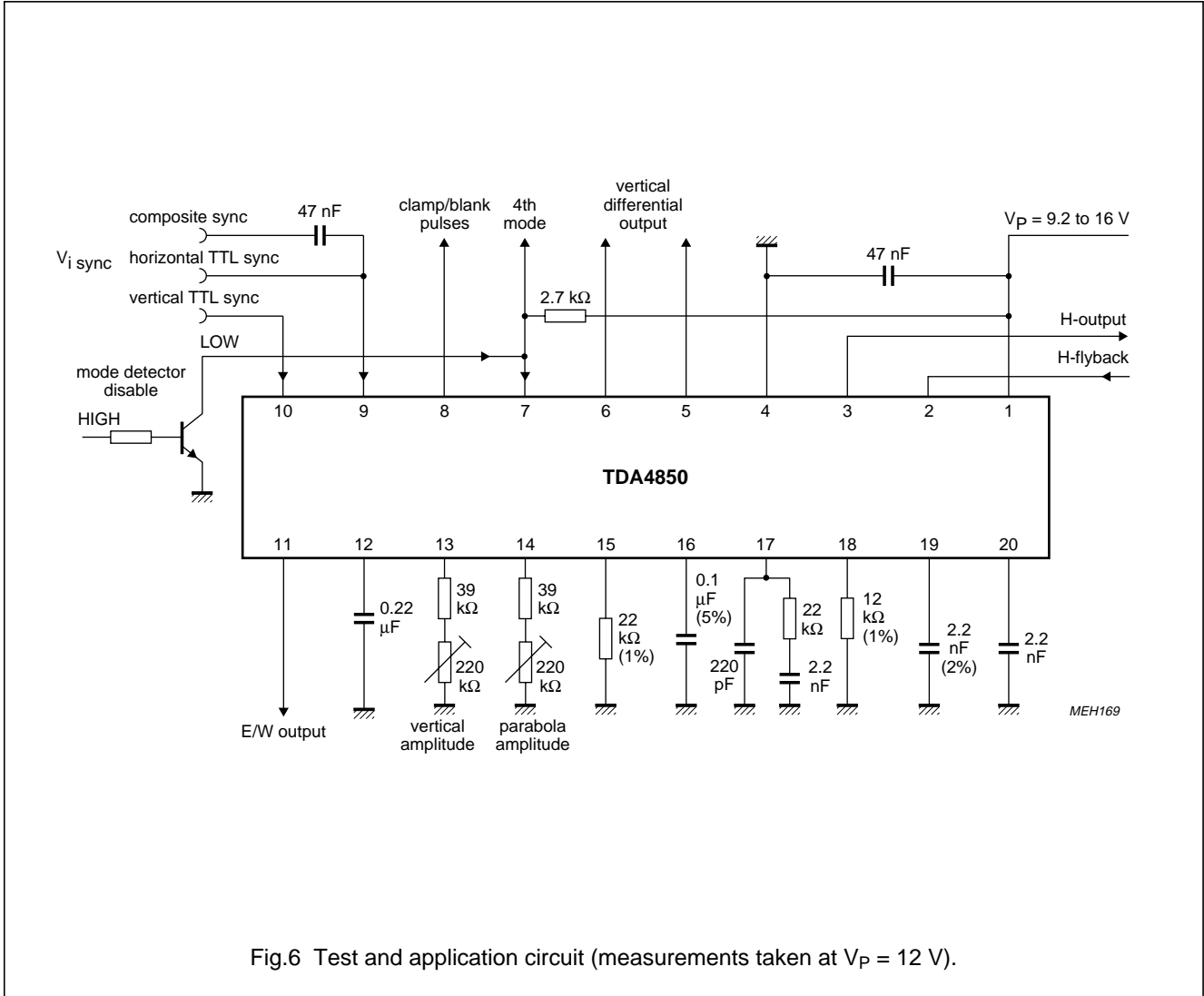


Fig.6 Test and application circuit (measurements taken at $V_P = 12 \text{ V}$).

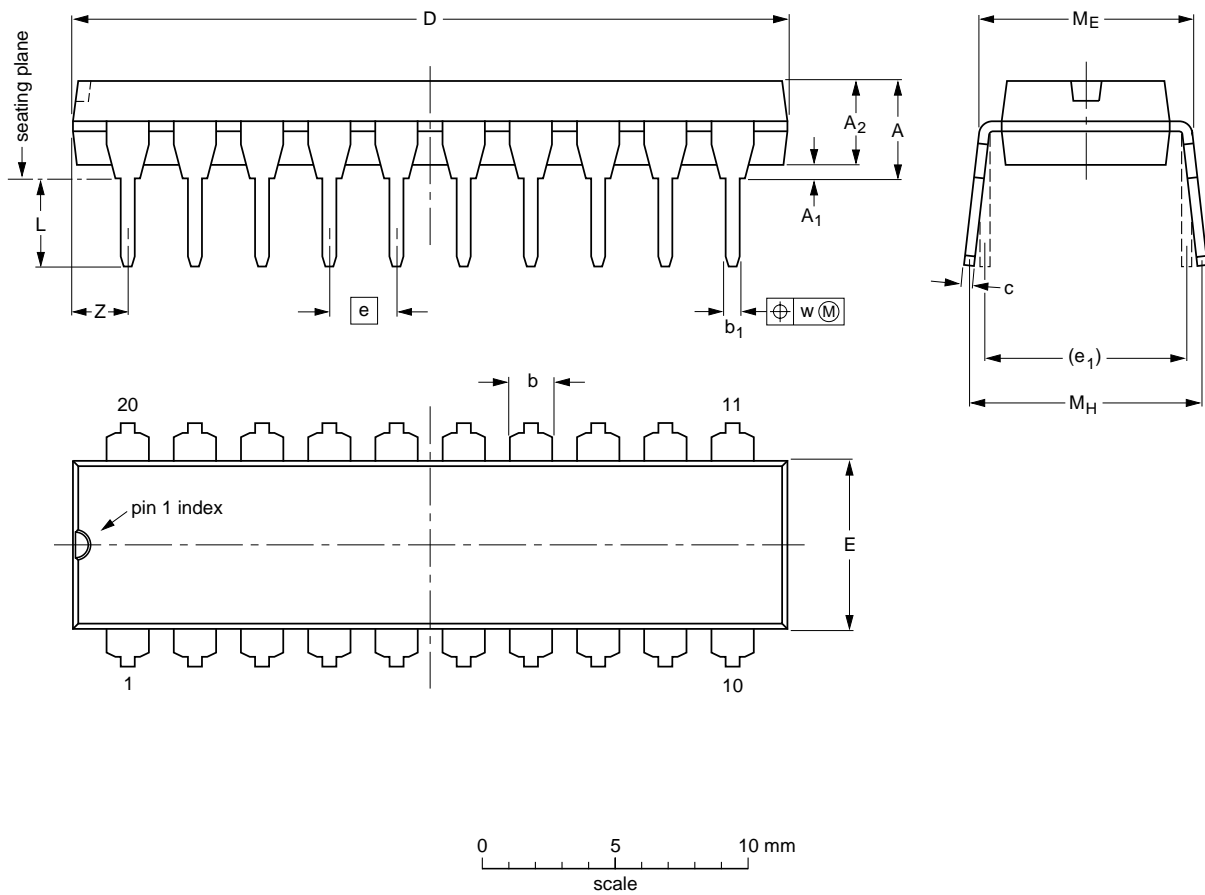
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PACKAGE OUTLINE

DIP20: plastic dual in-line package; 20 leads (300 mil)

SOT146-1



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

UNIT	A max.	A ₁ min.	A ₂ max.	b	b ₁	c	D ⁽¹⁾	E ⁽¹⁾	e	e ₁	L	M _E	M _H	w	Z ⁽¹⁾ max.
mm	4.2	0.51	3.2	1.73 1.30	0.53 0.38	0.36 0.23	26.92 26.54	6.40 6.22	2.54	7.62	3.60 3.05	8.25 7.80	10.0 8.3	0.254	2.0
inches	0.17	0.020	0.13	0.068 0.051	0.021 0.015	0.014 0.009	1.060 1.045	0.25 0.24	0.10	0.30	0.14 0.12	0.32 0.31	0.39 0.33	0.01	0.078

Note

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT146-1			SC603			92-11-17 95-05-24