

IR2112(S) & (PbF)

HIGH AND LOW SIDE DRIVER

Features

- Floating channel designed for bootstrap operation
 - Fully operational to +600V
 - Tolerant to negative transient voltage dV/dt immune
 - Gate drive supply range from 10 to 20V
 - Undervoltage lockout for both channels
 - 3.3V logic compatible
- Separate logic supply range from 3.3V to 20V
Logic and power ground $\pm 5V$ offset
- CMOS Schmitt-triggered inputs with pull-down
 - Cycle by cycle edge-triggered shutdown logic
 - Matched propagation delay for both channels
 - Outputs in phase with inputs
 - Also available LEAD-FREE

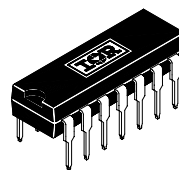
Description

The IR2112(S) is a high voltage, high speed power MOSFET and IGBT driver with independent high and low side referenced output channels. Proprietary HVIC and latch immune CMOS technologies enable ruggedized monolithic construction. Logic inputs are compatible with standard CMOS or LSTTL outputs, down to 3.3V logic. The output drivers feature a high pulse current buffer stage designed for minimum driver cross-conduction. Propagation delays are matched to simplify use in high frequency applications. The floating channel can be used to drive an N-channel power MOSFET or IGBT in the high side configuration which operates up to 600 volts.

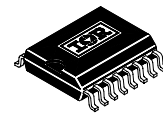
Product Summary

V _{OFFSET}	600V max.
I _{O+/-}	200 mA / 420 mA
V _{OUT}	10 - 20V
t _{on/off} (typ.)	125 & 105 ns
Delay Matching	30 ns

Packages

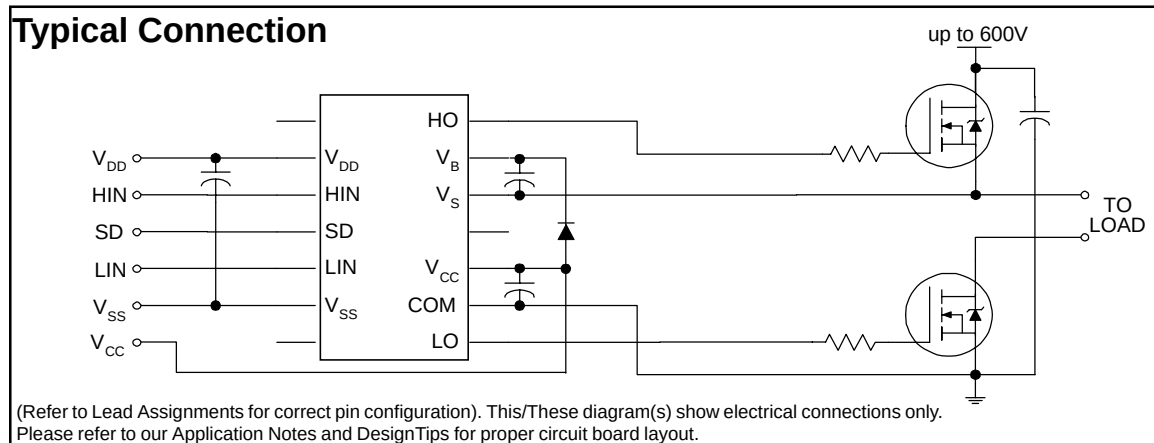


14-Lead PDIP



16-Lead SOIC
(wide body)

Typical Connection



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Absolute Maximum Ratings

Absolute Maximum Ratings indicate sustained limits beyond which damage to the device may occur. All voltage parameters are absolute voltages referenced to COM. The Thermal Resistance and Power Dissipation ratings are measured under board mounted and still air conditions. Additional information is shown in Figures 28 through 35.

Symbol	Definition	Min.	Max.	Units
V_B	High Side Floating Supply Voltage	-0.3	625	V
V_S	High Side Floating Supply Offset Voltage	$V_B - 25$	$V_B + 0.3$	
V_{HO}	High Side Floating Output Voltage	$V_S - 0.3$	$V_B + 0.3$	
V_{CC}	Low Side Fixed Supply Voltage	-0.3	25	
V_{LO}	Low Side Output Voltage	-0.3	$V_{CC} + 0.3$	
V_{DD}	Logic Supply Voltage	-0.3	$V_{SS} + 25$	
V_{SS}	Logic Supply Offset Voltage	$V_{CC} - 25$	$V_{CC} + 0.3$	
V_{IN}	Logic Input Voltage (HIN, LIN & SD)	$V_{SS} - 0.3$	$V_{DD} + 0.3$	
dV_S/dt	Allowable Offset Supply Voltage Transient (Figure 2)	—	50	V/ns
P_D	Package Power Dissipation @ $T_A \leq +25^\circ\text{C}$ (14 Lead DIP)	—	1.6	W
	(16 Lead SOIC)	—	1.25	
R_{THJA}	Thermal Resistance, Junction to Ambient (14 Lead DIP)	—	75	$^\circ\text{C/W}$
	(16 Lead SOIC)	—	100	
T_J	Junction Temperature	—	150	$^\circ\text{C}$
T_S	Storage Temperature	-55	150	
T_L	Lead Temperature (Soldering, 10 seconds)	—	300	

Recommended Operating Conditions

The Input/Output logic timing diagram is shown in Figure 1. For proper operation the device should be used within the recommended conditions. The V_S and V_{SS} offset ratings are tested with all supplies biased at 15V differential. Typical ratings at other bias conditions are shown in Figures 36 and 37.

Symbol	Definition	Min.	Max.	Units
V_B	High Side Floating Supply Absolute Voltage	$V_S + 10$	$V_S + 20$	V
V_S	High Side Floating Supply Offset Voltage	Note 1	600	
V_{HO}	High Side Floating Output Voltage	V_S	V_B	
V_{CC}	Low Side Fixed Supply Voltage	10	20	
V_{LO}	Low Side Output Voltage	0	V_{CC}	
V_{DD}	Logic Supply Voltage	$V_{SS} + 3$	$V_{SS} + 20$	
V_{SS}	Logic Supply Offset Voltage	-5 (Note 2)	5	
V_{IN}	Logic Input Voltage (HIN, LIN & SD)	V_{SS}	V_{DD}	
T_A	Ambient Temperature	-40	125	$^\circ\text{C}$

Note 1: Logic operational for V_S of -5 to +600V. Logic state held for V_S of -5V to $-V_{BS}$. (Please refer to the Design Tip DT97-3 for more details).

Note 2: When $V_{DD} < 5V$, the minimum V_{SS} offset is limited to $-V_{DD}$.

Dynamic Electrical Characteristics

V_{BIAS} (V_{CC} , V_{BS} , V_{DD}) = 15V, C_L = 1000 pF, T_A = 25°C and V_{SS} = COM unless otherwise specified. The dynamic electrical characteristics are measured using the test circuit shown in Figure 3.

Symbol	Definition	Figure	Min.	Typ.	Max.	Units	Test Conditions
t_{on}	Turn-On Propagation Delay	7	—	125	180	ns	$V_S = 0V$
t_{off}	Turn-Off Propagation Delay	8	—	105	160		$V_S = 600V$
t_{sd}	Shutdown Propagation Delay	9	—	105	160		$V_S = 600V$
t_r	Turn-On Rise Time	10	—	80	130		
t_f	Turn-Off Fall Time	11	—	40	65		
MT	Delay Matching, HS & LS Turn-On/Off	—	—	—	30		

Static Electrical Characteristics

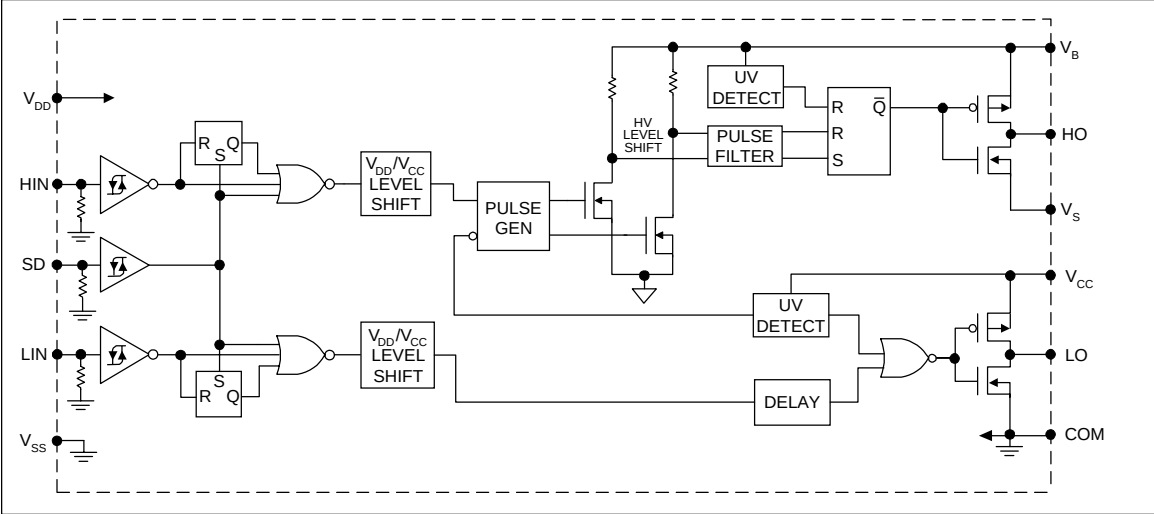
V_{BIAS} (V_{CC} , V_{BS} , V_{DD}) = 15V, T_A = 25°C and V_{SS} = COM unless otherwise specified. The V_{IN} , V_{TH} and I_{IN} parameters are referenced to V_{SS} and are applicable to all three logic input leads: HIN, LIN and SD. The V_O and I_O parameters are referenced to COM and are applicable to the respective output leads: HO or LO.

Symbol	Definition	Figure	Min.	Typ.	Max.	Units	Test Conditions
V_{IH}	Logic "1" Input Voltage	12	9.5	—	—	V	
V_{IL}	Logic "0" Input Voltage	13	—	—	6.0		
V_{OH}	High Level Output Voltage, $V_{BIAS} - V_O$	14	—	—	100	mV	$I_O = 0A$
V_{OL}	Low Level Output Voltage, V_O	15	—	—	100		$I_O = 0A$
I_{LK}	Offset Supply Leakage Current	16	—	—	50	μA	$V_B = V_S = 600V$
I_{QBS}	Quiescent V_{BS} Supply Current	17	—	25	60		$V_{IN} = 0V$ or V_{DD}
I_{QCC}	Quiescent V_{CC} Supply Current	18	—	80	180		$V_{IN} = 0V$ or V_{DD}
I_{QDD}	Quiescent V_{DD} Supply Current	19	—	2.0	5.0		$V_{IN} = 0V$ or V_{DD}
I_{IN+}	Logic "1" Input Bias Current	20	—	20	40		$V_{IN} = V_{DD}$
I_{IN-}	Logic "0" Input Bias Current	21	—	—	1.0		$V_{IN} = 0V$
V_{BSUV+}	V_{BS} Supply Undervoltage Positive Going Threshold	22	7.4	8.5	9.6	V	
V_{BSUV-}	V_{BS} Supply Undervoltage Negative Going Threshold	23	7.0	8.1	9.2		
V_{CCUV+}	V_{CC} Supply Undervoltage Positive Going Threshold	24	7.6	8.6	9.6		
V_{CCUV-}	V_{CC} Supply Undervoltage Negative Going Threshold	25	7.2	8.2	9.2		
I_{O+}	Output High Short Circuit Pulsed Current	26	200	250	—	mA	$V_O = 0V$, $V_{IN} = V_{DD}$ $PW \leq 10 \mu s$
I_{O-}	Output Low Short Circuit Pulsed Current	27	420	500	—		$V_O = 15V$, $V_{IN} = 0V$ $PW \leq 10 \mu s$

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Functional Block Diagram



Lead Definitions

Symbol	Description
VDD	Logic supply
HIN	Logic input for high side gate driver output (HO), in phase
SD	Logic input for shutdown
LIN	Logic input for low side gate driver output (LO), in phase
VSS	Logic ground
VB	High side floating supply
HO	High side gate drive output
VS	High side floating supply return
VCC	Low side supply
LO	Low side gate drive output
COM	Low side return

Lead Assignments

14 Lead DIP	16 Lead SOIC (Wide Body)
IR2112	IR2112S
Part Number	

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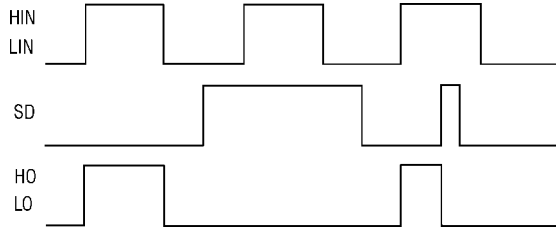


Figure 1. Input/Output Timing Diagram

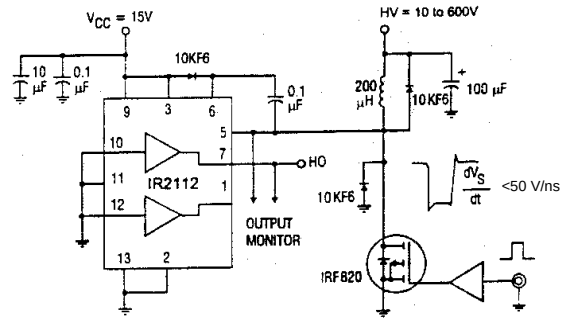


Figure 2. Floating Supply Voltage Transient Test Circuit

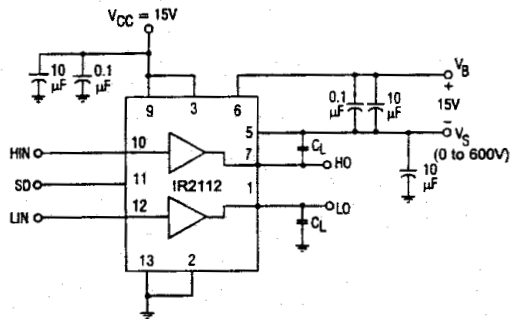


Figure 3. Switching Time Test Circuit

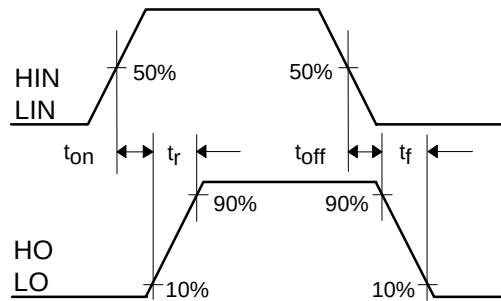


Figure 4. Switching Time Waveform Definition

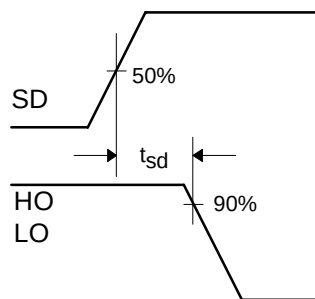


Figure 5. Shutdown Waveform Definitions

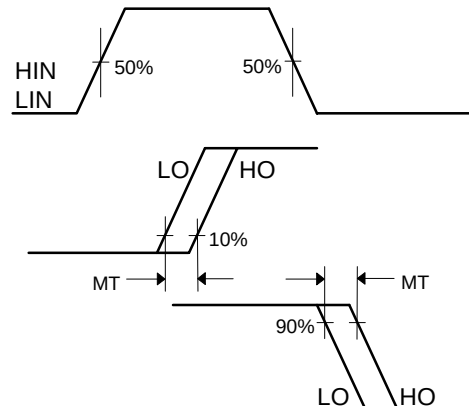


Figure 6. Delay Matching Waveform Definitions

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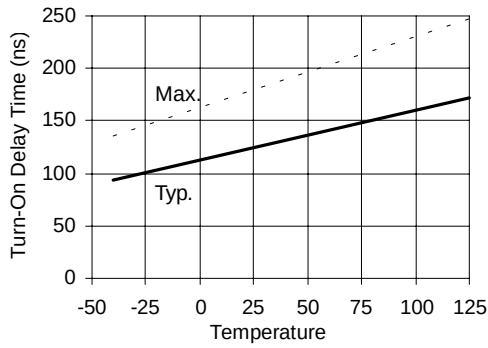


Figure 7A. Turn-On Time vs. Temperature

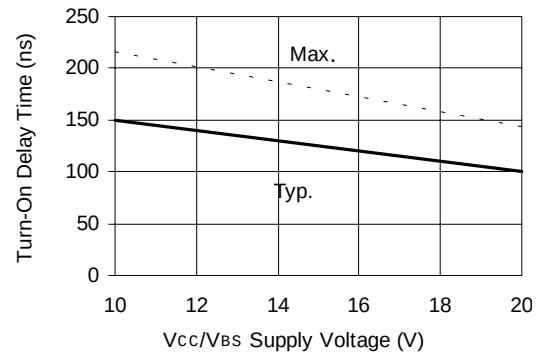


Figure 7B. Turn-On Time vs. Vcc/Vbs Supply Voltage

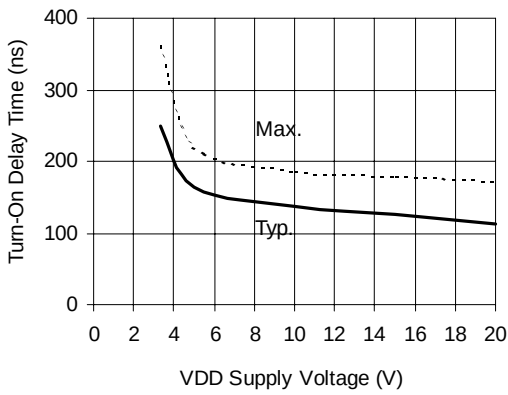


Figure 7C. Turn-On Time vs. VDD Supply Voltage

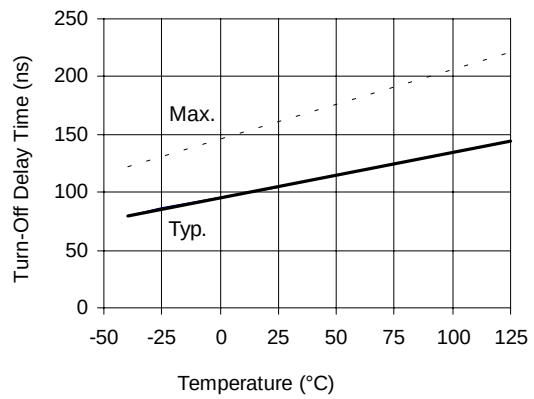


Figure 8A. Turn-Off Time vs. Temperature

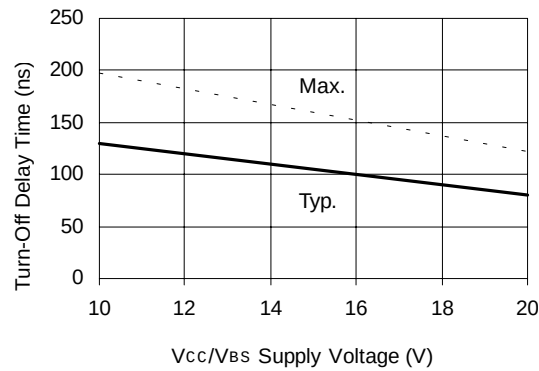


Figure 8B. Turn-Off Time vs. Vcc/Vbs Supply Voltage

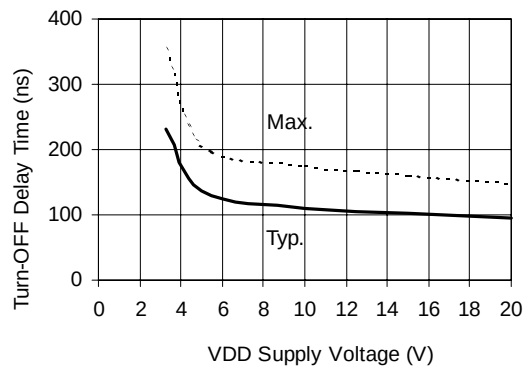


Figure 8C. Turn-Off Time vs. VDD Supply Voltage

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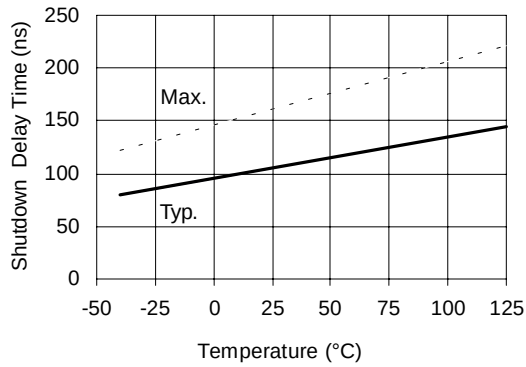


Figure 9A. Shutdown Time vs. Temperature

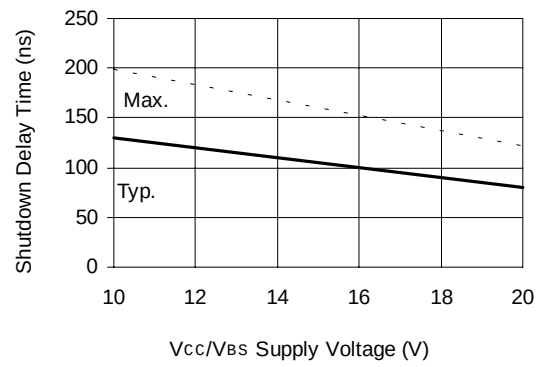


Figure 9B. Shutdown Delay Time vs. Vcc/Vbs Supply Voltage

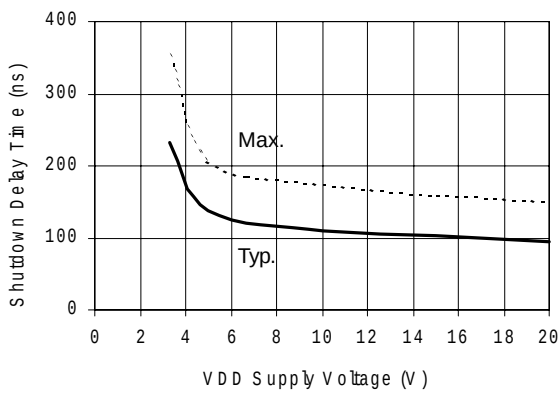


Figure 9C. Shutdown Time vs. VDD Supply Voltage

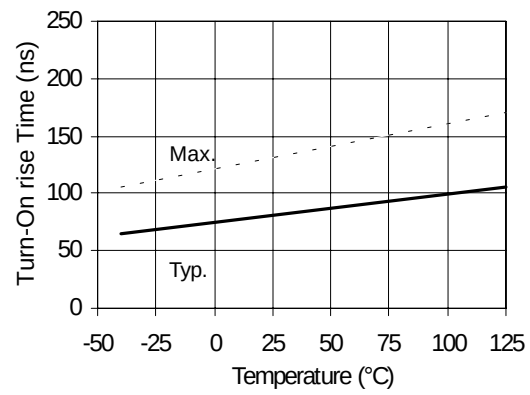


Figure 10A. Turn-On Rise Time vs. Temperature

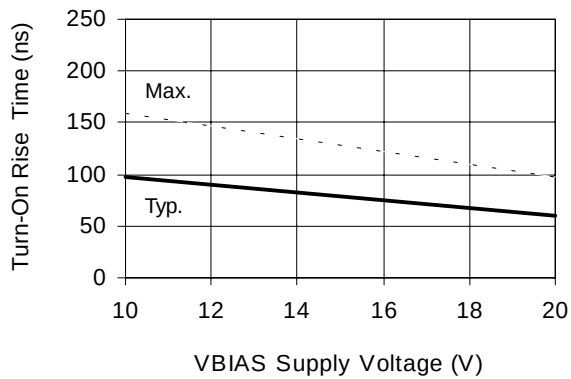


Figure 10B. Turn-On Rise Time vs. Voltage

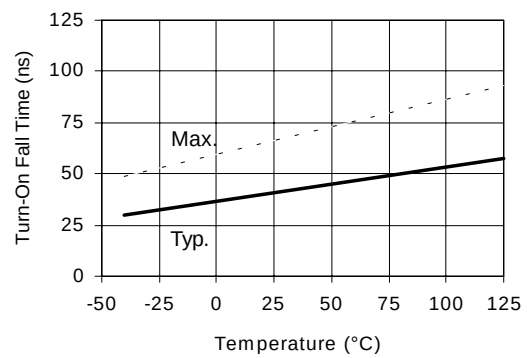


Figure 11A Turn-On Fall Time vs. Temperature

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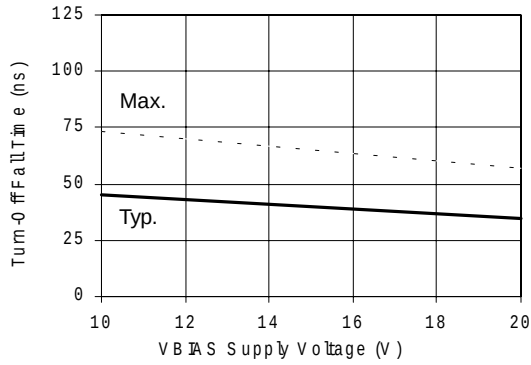


Figure 11B. Turn-Off Fall Time vs. Voltage

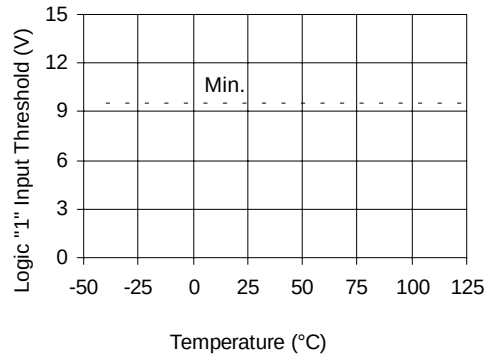


Figure 12A. Logic "1" Input Threshold vs. Temperature

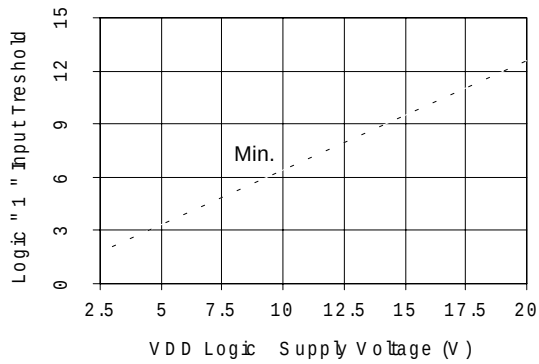


Figure 12B. Logic "1" Input Threshold vs. Voltage

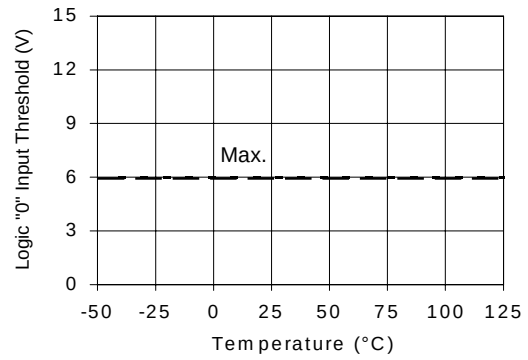


Figure 13A. Logic "0" Input Threshold vs. Temperature

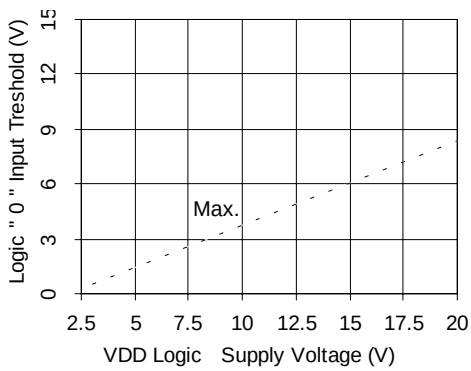


Figure 13B. Logic "0" Input Threshold vs. Voltage

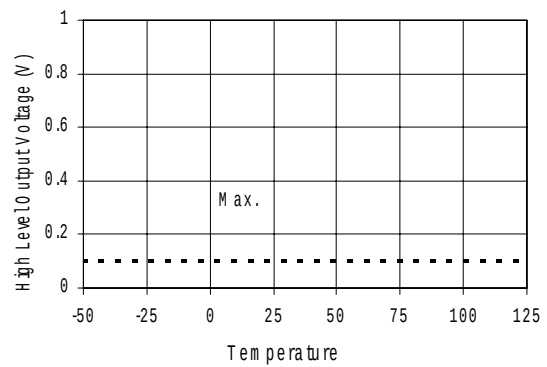


Figure 14A. High Level Output vs. Temperature

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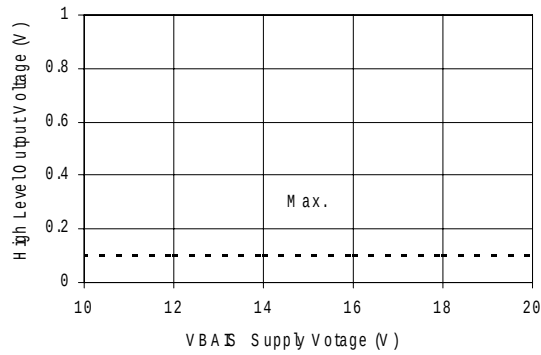


Figure 14B. High Level Output vs. Voltage

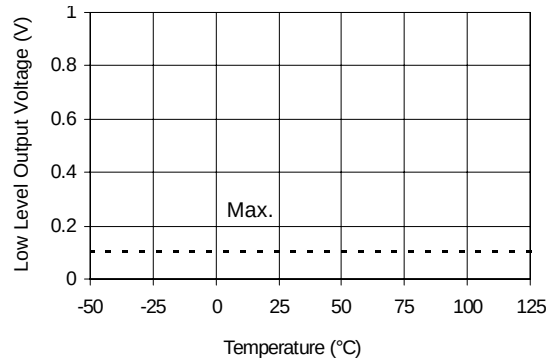


Figure 15A. Low Level Output vs. Temperature

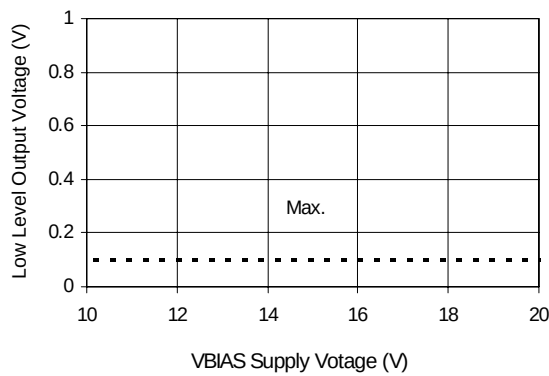


Figure 15B. Low Level Output vs. Voltage

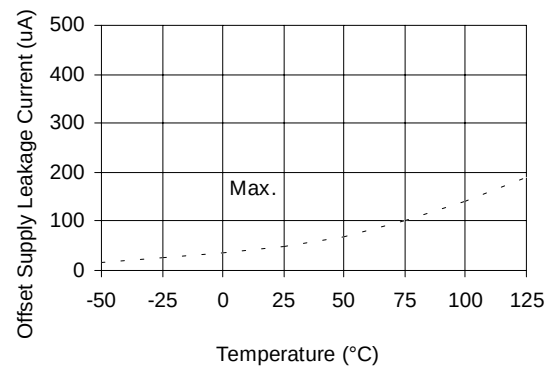


Figure 16A. Offset Supply Current vs. Temperature

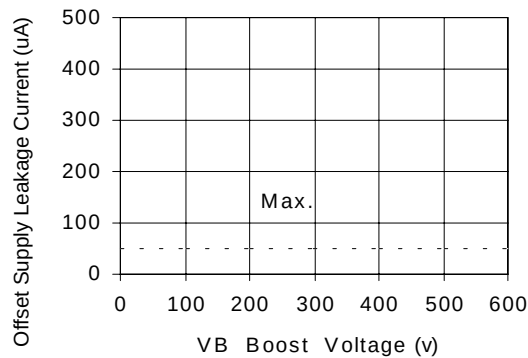


Figure 16B. Offset Supply Current vs. Voltage

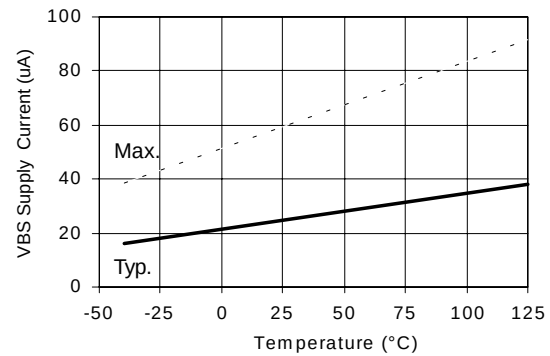


Figure 17A. Vbs Supply Current vs. Temperature

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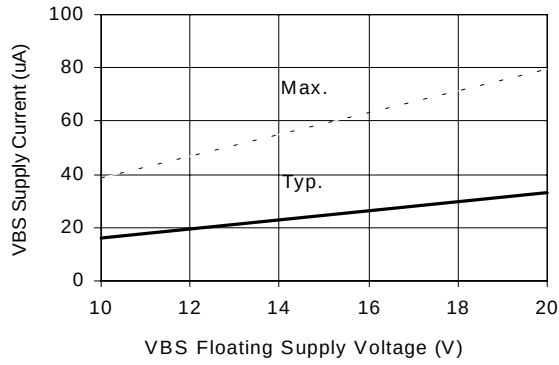


Figure 17B. VBS Supply Current vs. Voltage

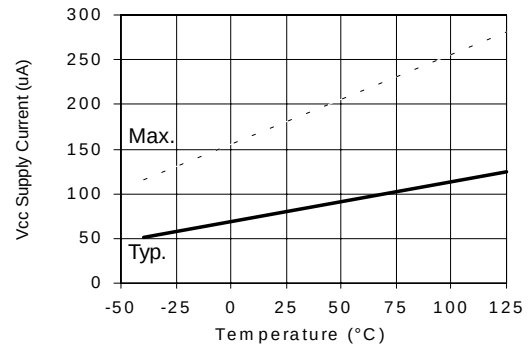


Figure 18A. VCC Supply Current vs. Temperature

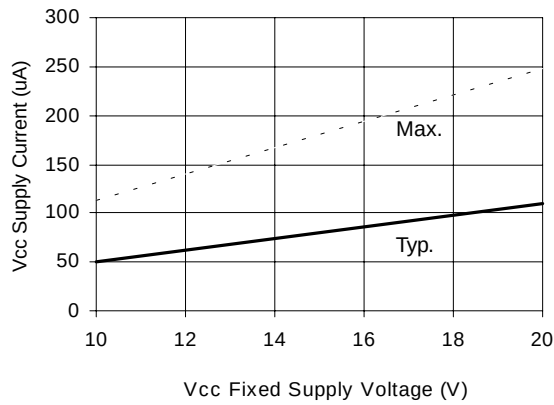


Figure 18B. VCC Supply Current vs. Voltage

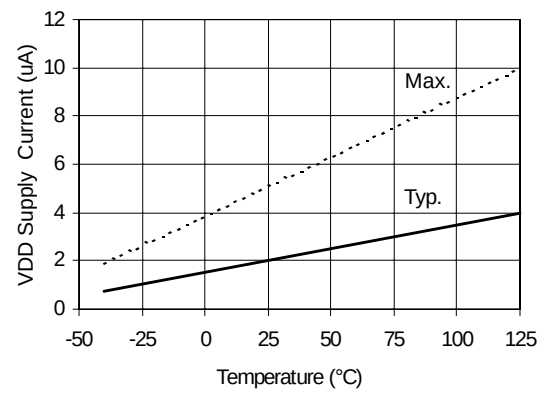


Figure 19A. VDD Supply Current vs. Temperature

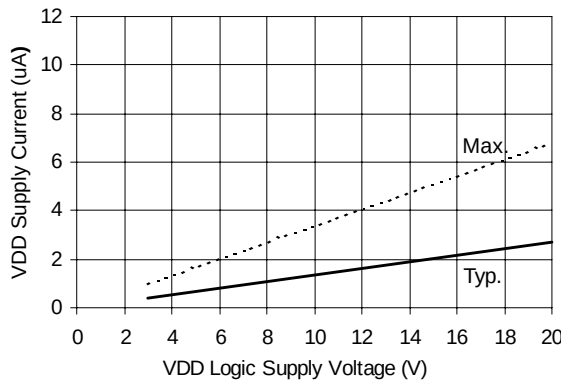


Figure 19B. VDD Supply Current vs. VDD Voltage

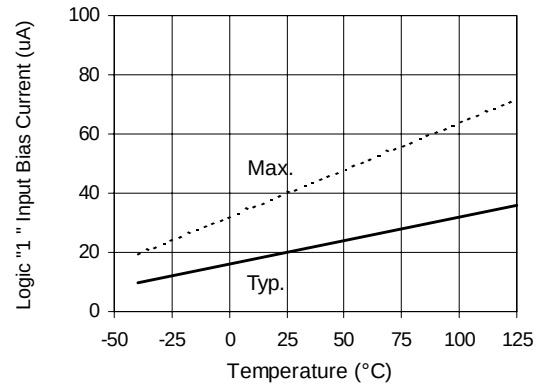


Figure 20A. Logic "1" Input Current vs. Temperature

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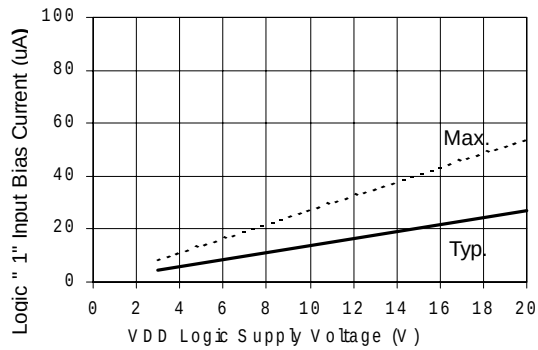


Figure 20B. Logic "1" Input Current vs. V_{DD} Voltage

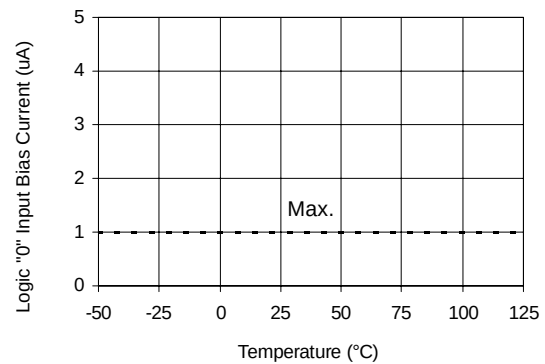


Figure 21A. Logic "0" Input Current vs. Temperature

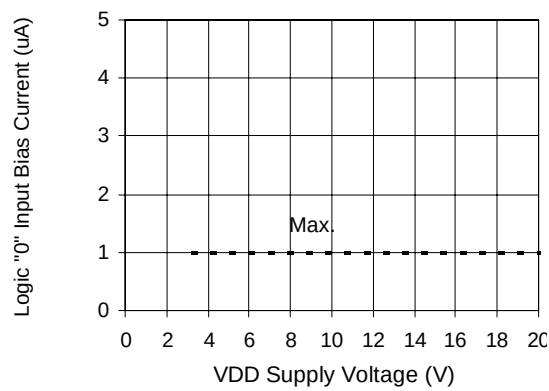


Figure 21B. Logic "0" Input Current vs. V_{DD} Voltage

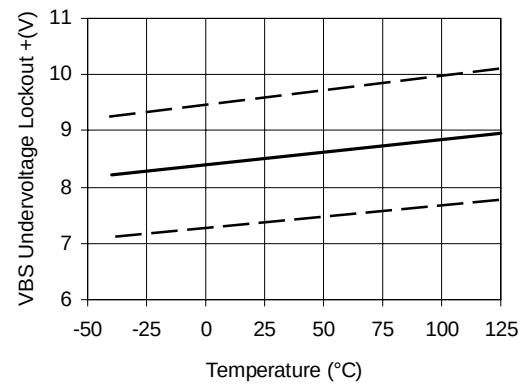


Figure 22. V_{BS} Undervoltage (+) vs. Temperature

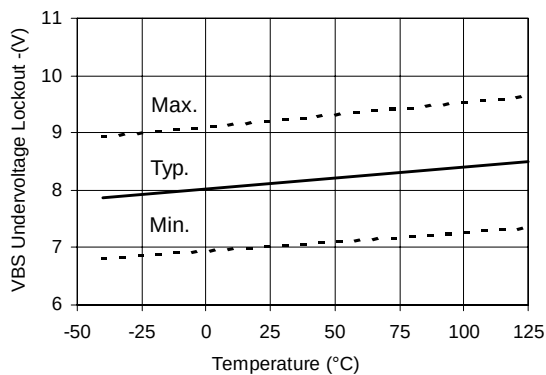


Figure 23. V_{BS} Undervoltage (-) vs. Temperature

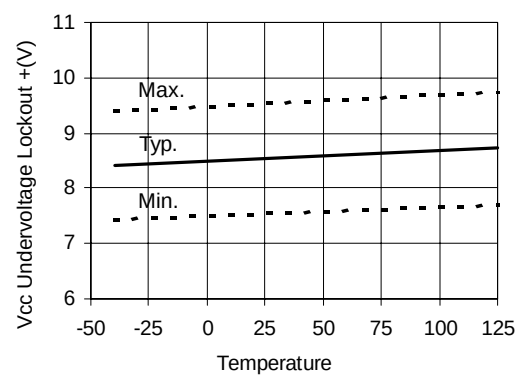


Figure 24. V_{CC} Undervoltage (-) vs. Temperature

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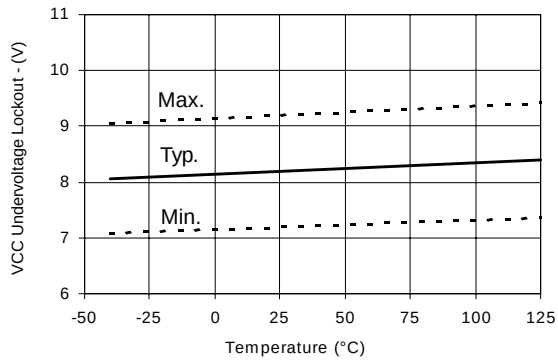


Figure 25. VCC Undervoltage (-) vs. Temperature

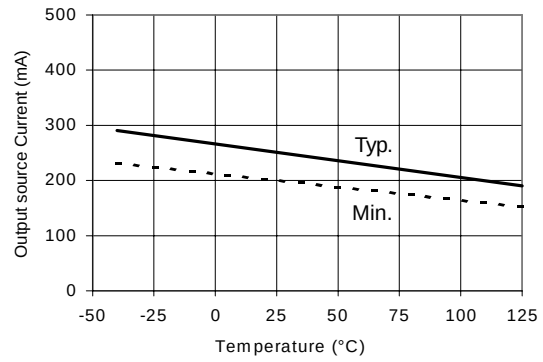


Figure 26A. Output Source Current vs. Temperature

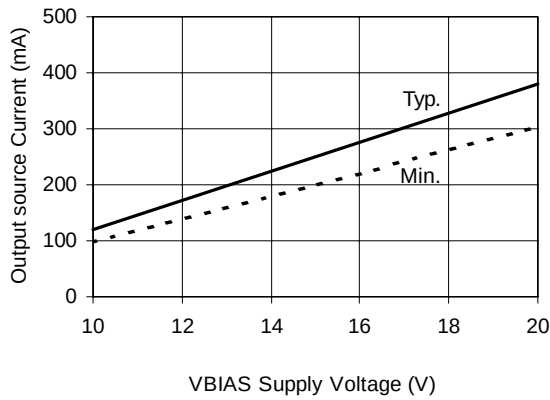


Figure 26B. Output Source Current vs. Voltage

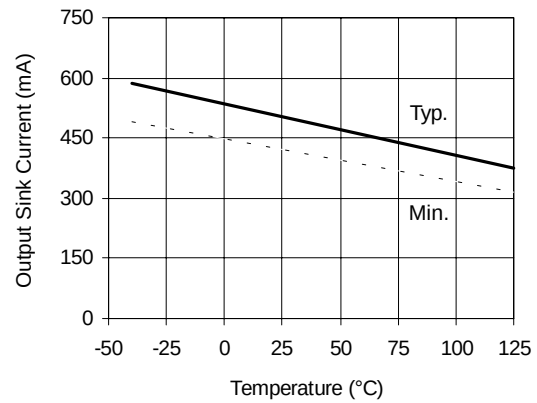


Figure 27A. Output Sink Current vs. Temperature

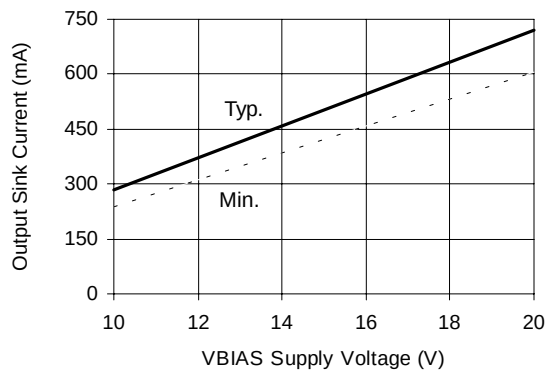


Figure 27B. Output Sink Current vs. Voltage

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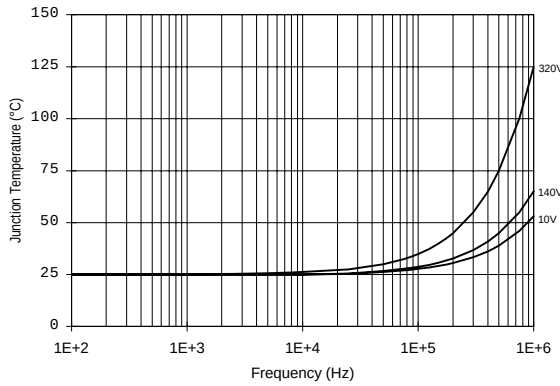


Figure 28. IR2112 T_J vs. Frequency (IRFBC20)
 $R_{GATE} = 33\Omega$, $V_{CC} = 15V$

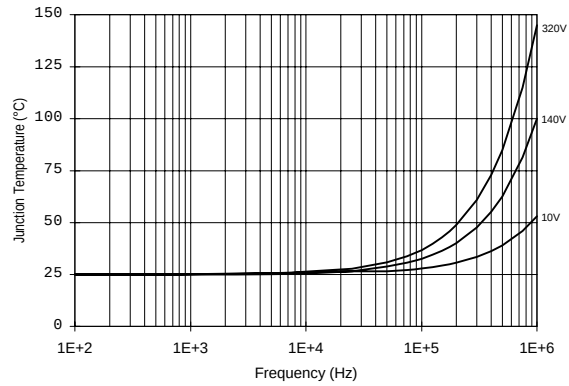


Figure 29. IR2112 T_J vs. Frequency (IRFBC30)
 $R_{GATE} = 22\Omega$, $V_{CC} = 15V$

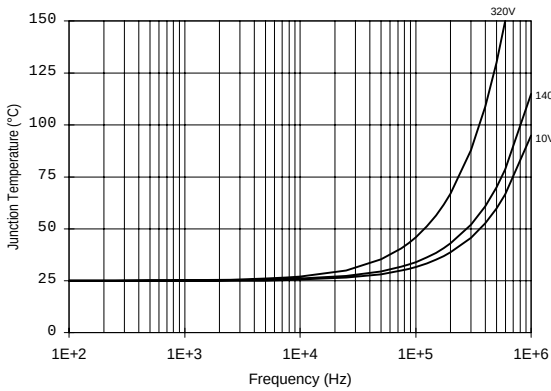


Figure 30. IR2112 T_J vs. Frequency (IRFBC40)
 $R_{GATE} = 15\Omega$, $V_{CC} = 15V$

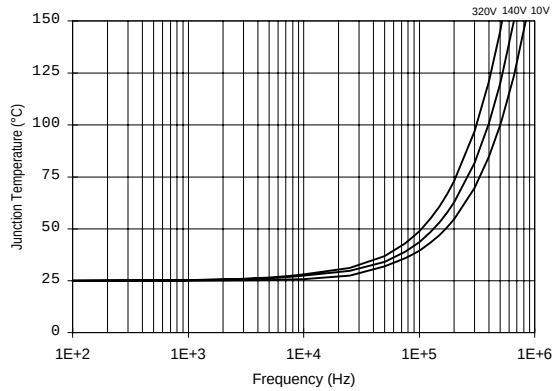


Figure 31. IR2112 T_J vs. Frequency (IRFPE50)
 $R_{GATE} = 10\Omega$, $V_{CC} = 15V$

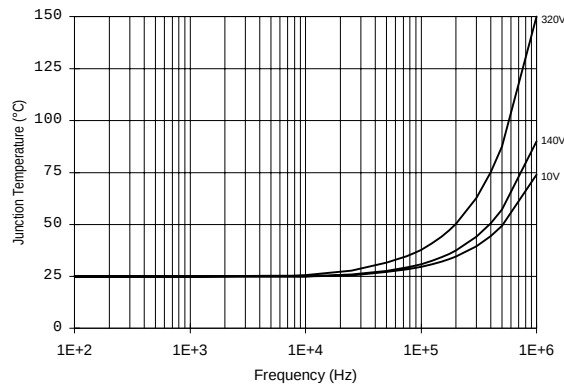


Figure 32. IR2112S T_J vs. Frequency (IRFBC20)
 $R_{GATE} = 33\Omega$, $V_{CC} = 15V$

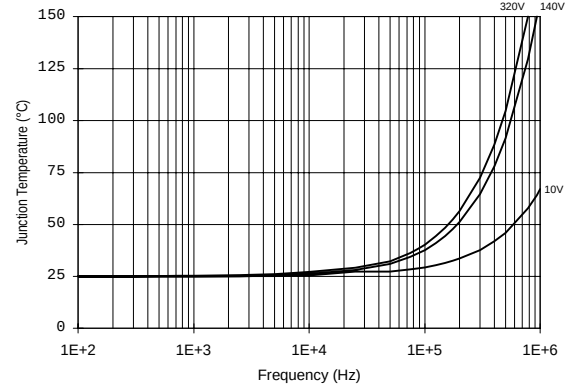


Figure 33. IR2112S T_J vs. Frequency (IRFBC30)
 $R_{GATE} = 22\Omega$, $V_{CC} = 15V$

IR2112(S) & (PbF)

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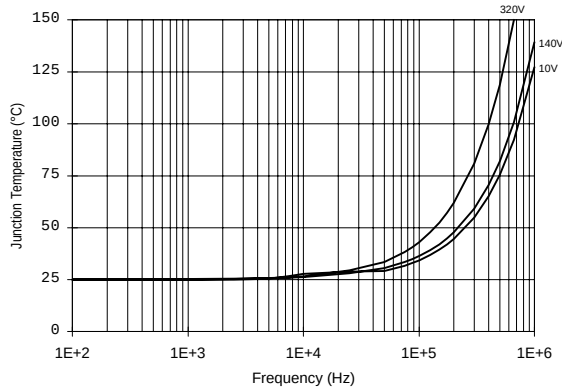


Figure 34. IR2112S T_J vs. Frequency (IRFBC40)
 $R_{GATE} = 15\Omega$, $V_{CC} = 15V$

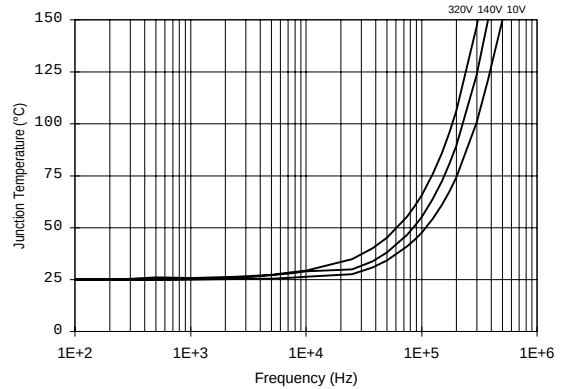


Figure 35. IR2112S T_J vs. Frequency (IRFPE50)
 $R_{GATE} = 10\Omega$, $V_{CC} = 15V$

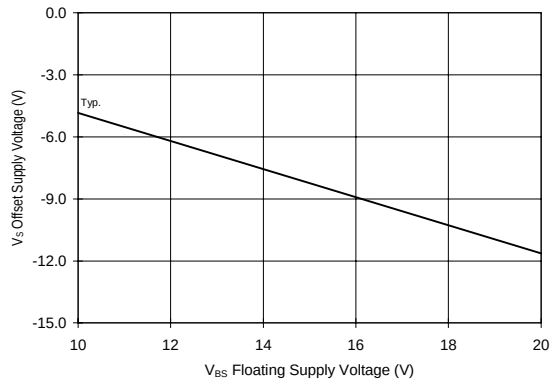


Figure 36. Maximum V_S Negative Offset vs. V_{BS} Supply Voltage

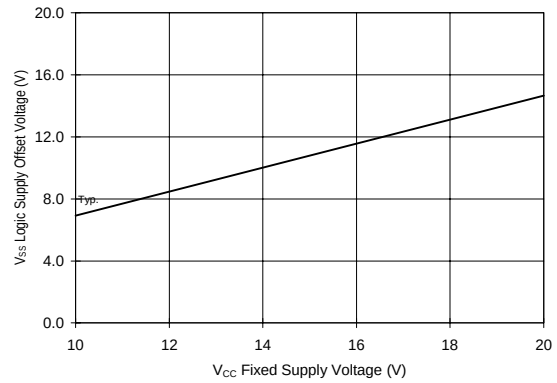
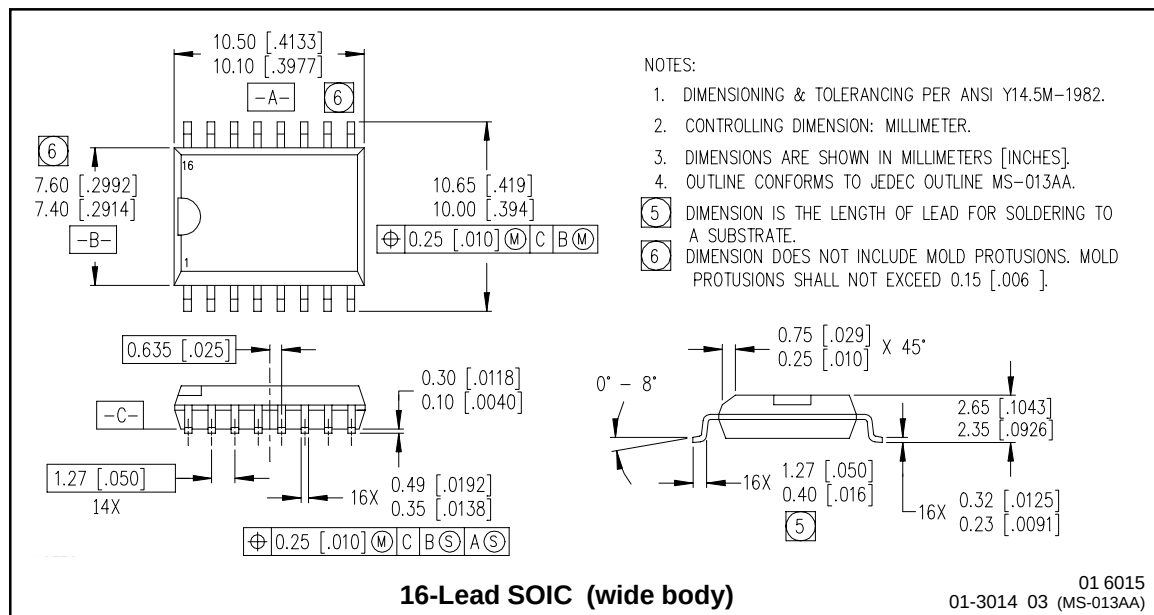
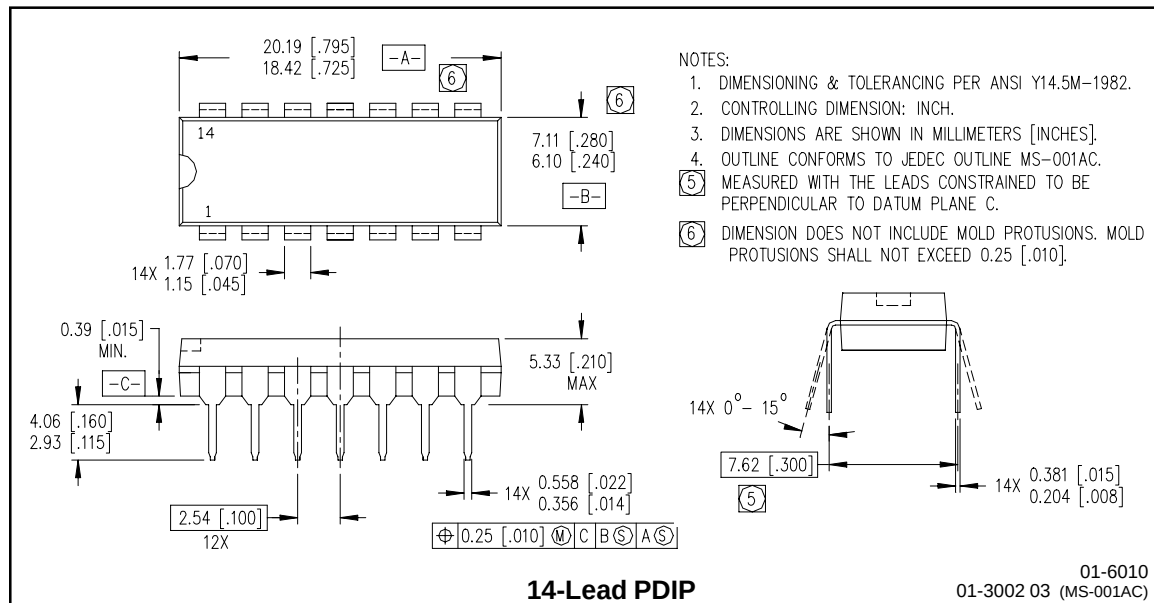


Figure 37. Maximum V_{SS} Positive Offset vs. V_{CC} Supply Voltage

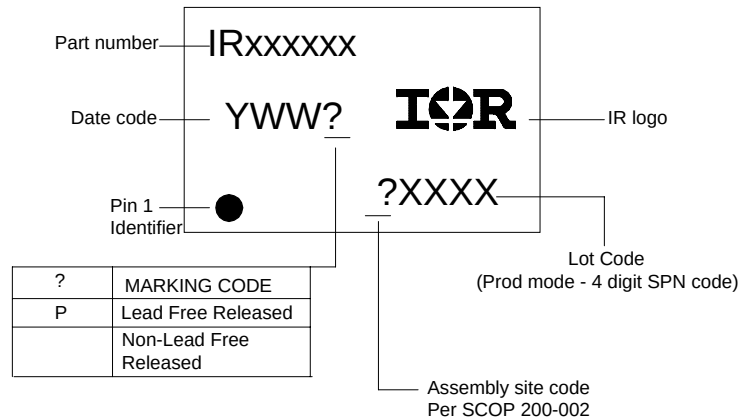
Case outline



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LEADFREE PART MARKING INFORMATION



ORDER INFORMATION

Basic Part (Non-Lead Free)

14-Lead PDIP IR2112 order IR2112
16-Lead SOIC IR2112S order IR2112S

Leadfree Part

14-Lead PDIP IR2112 order IR2112PbF
16-Lead SOIC IR2112S order IR2112SPbF

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This product has been qualified per industrial level

Data and specifications subject to change without notice. 4/2/2004